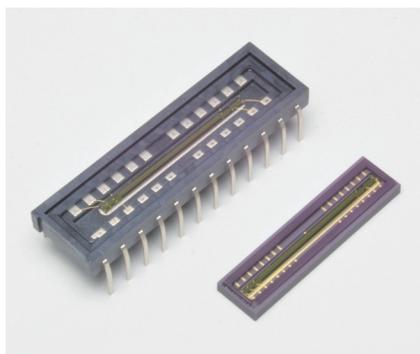


# CMOS linear image sensors



S15796 series

## High sensitivity, photosensitive area with vertically long pixels

The S15796 series is a high sensitivity CMOS linear image sensor using a photosensitive area with vertically long pixels ( $7 \times 200 \mu\text{m}$ ). Other features include high sensitivity and high resistance in the UV region. The S15796 series operates from a single 5 V supply making it suitable for use in low cost spectrometers. The S15796-1024-20 and S15796-2048-20 are provided in a surface mount type package.

### Features

- Pixel size:  $7 \times 200 \mu\text{m}$
- Effective photosensitive area length: 7.168 mm (1024 pixels)  
: 14.336 mm (2048 pixels)
- High sensitivity:  $650 \text{ V}/(\text{lx}\cdot\text{s})$
- High sensitivity in the UV to NIR region  
(spectral response range: 200 to 1000 nm)
- Simultaneous charge integration for all pixels
- Variable integration time function  
(electronic shutter function)
- 5 V single power supply operation
- Built-in timing generator allows operation with only  
start and clock pulse inputs
- Video data rate: 10 MHz max.

### Applications

- Spectrophotometry
- Position detection
- Image reading
- Encoders

### Structure

Parameter	S15796-1024	S15796-1024-20	S15796-2048	S15796-2048-20	Unit	
Number of pixels	1024		2048		-	
Pixel size	$7 \times 200$					$\mu\text{m}$
Photosensitive area length	7.168		14.336		mm	
Package	LCP (liquid crystal polymer)	Surface mount type ceramic	LCP (liquid crystal polymer)	Surface mount type ceramic	-	
Window material	Quartz					-

### Absolute maximum ratings

Parameter	Symbol	Condition	S15796-1024 S15796-2048	S15796-1024-20 S15796-2048-20	Unit
Supply voltage	Vdd	Ta=25 °C	-0.3 to +6		V
Clock pulse voltage	V(CLK)	Ta=25 °C	-0.3 to +6		V
Start pulse voltage	V(ST)	Ta=25 °C	-0.3 to +6		V
Operating temperature	Topr	No dew condensation*1	-40 to +65		°C
Storage temperature	Tstg	No dew condensation*1	-40 to +65		°C
Soldering temperature	Tsol		*2	260 (twice)*3	°C

\*1: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

\*2: See the recommended soldering conditions (P.14).

\*3: Reflow soldering, IPC/JEDEC J-STD-020 MSL2a, see P.14

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

### ▣ Recommended terminal voltage (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Vdd	4.75	5	5.25	V
Clock pulse voltage	High level	V(CLK)	3	Vdd	Vdd + 0.25	V
	Low level		0	-	0.3	
Start pulse voltage	High level	V(ST)	3	Vdd	Vdd + 0.25	V
	Low level		0	-	0.3	

### ▣ Input terminal capacitance (Ta=25 °C, Vdd=5 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse input terminal capacitance	C(CLK)	-	5	-	pF
Start pulse input terminal capacitance	C(ST)	-	5	-	pF

### ▣ Electrical characteristics [Ta=25 °C, Vdd=5 V, V(CLK)=V(ST)=5 V]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse frequency	f(CLK)	200 k	-	10 M	Hz
Data rate	DR	-	f(CLK)	-	Hz
Output impedance	Zo	70	-	260	Ω
Current consumption*4 *5	-1024 series	15	25	35	mA
	-2048 series	20	30	40	

\*4: f(CLK)=10 MHz

\*5: Current consumption increases as the clock pulse frequency increases. The current consumption is 10 mA typ. at f(CLK)=200 kHz.

### ▣ Electrical and optical characteristics [Ta=25 °C, Vdd=5 V, V(CLK)=V(ST)=5 V, f(CLK)=10 MHz]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Spectral response range	λ	200 to 1000			nm
Peak sensitivity wavelength	λp	-	700	-	nm
Photosensitivity*6	Sw	-	650	-	V/(lx·s)
Conversion efficiency*7	CE	-	25	-	μV/e <sup>-</sup>
Dark output voltage*8	Vd	0	0.1	2.0	mV
Saturation output voltage*9 *10	Vsat	1.5	2.0	2.5	V
Readout noise	Nread	0.1	0.4	1.2	mV rms
Dynamic range 1*11	Drange1	-	5000	-	times
Dynamic range 2*12	Drange2	-	20000	-	times
Output offset voltage	Voffset	0.3	0.6	0.9	V
Photoresponse nonuniformity*6 *9 *13	PRNU	-	-	±10	%
Image lag*14	Lag	-	-	0.1	%

\*6: Measured with a tungsten lamp of 2856 K

\*7: Output voltage generated per electron

\*8: Integration time=10 ms

\*9: Voltage difference from Voffset

\*10: CDS (correlated double sampling) is done inside the image sensor in order to reduce noise. The final output is the difference between the output when the photosensitive area is put in the reset state, and the light output integrated in the photosensitive area. If used in an over-saturated state, the light output component may get mixed into the output when the photosensitive area is put in the reset state, causing the final output to decrease.

\*11:  $Drange1 = Vsat/Nread$

\*12:  $Drange2 = Vsat/Vd$

Integration time=10 ms

Dark output voltage is proportional to the integration time and so the shorter the integration time, the wider the dynamic range.

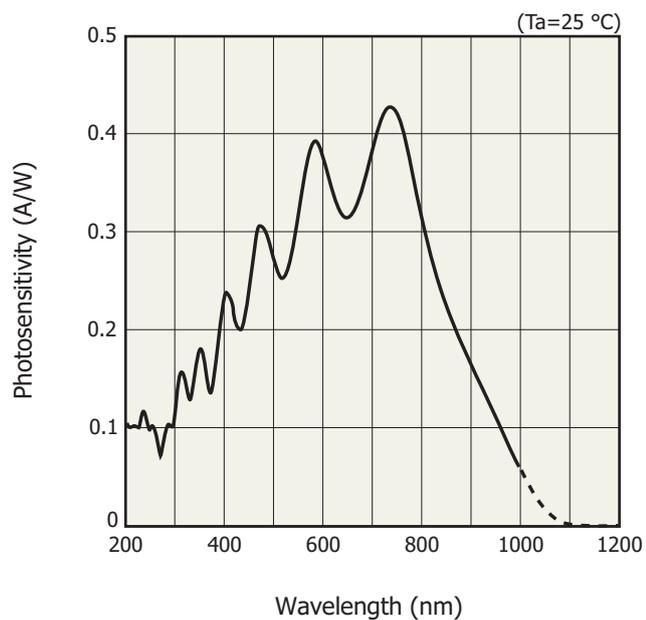
\*13: Photoresponse nonuniformity (PRNU) is the output nonuniformity that occurs when the entire photosensitive area is uniformly illuminated by light which is 50% of the saturation exposure level. PRNU is measured using 1018 pixels (S15796-1024 series) or 2042 pixels (S15796-2048 series) excluding 3 pixels each at both ends, and is defined as follows:

$$PRNU = \Delta X/X \times 100 (\%)$$

X: average of the output of all pixels, ΔX: difference between X and maximum output or minimum output

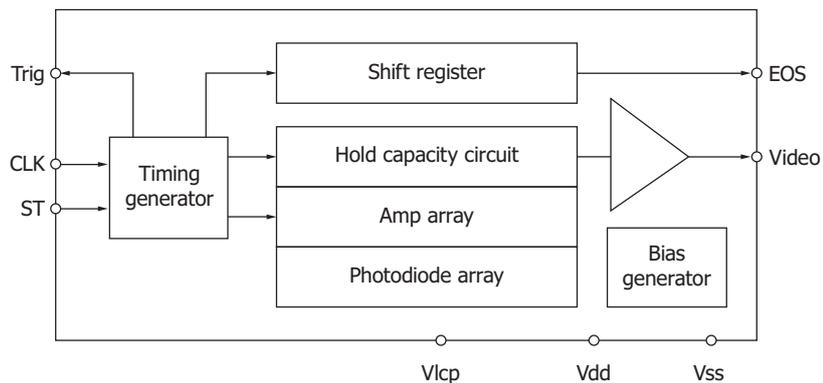
\*14: Signal components of the preceding line data that still remain even after the data is read out in a saturation output state. Image lag increases when the output exceeds the saturation output voltage.

**Spectral response (typical example)**



KMPDB0467EB

**Block diagram**

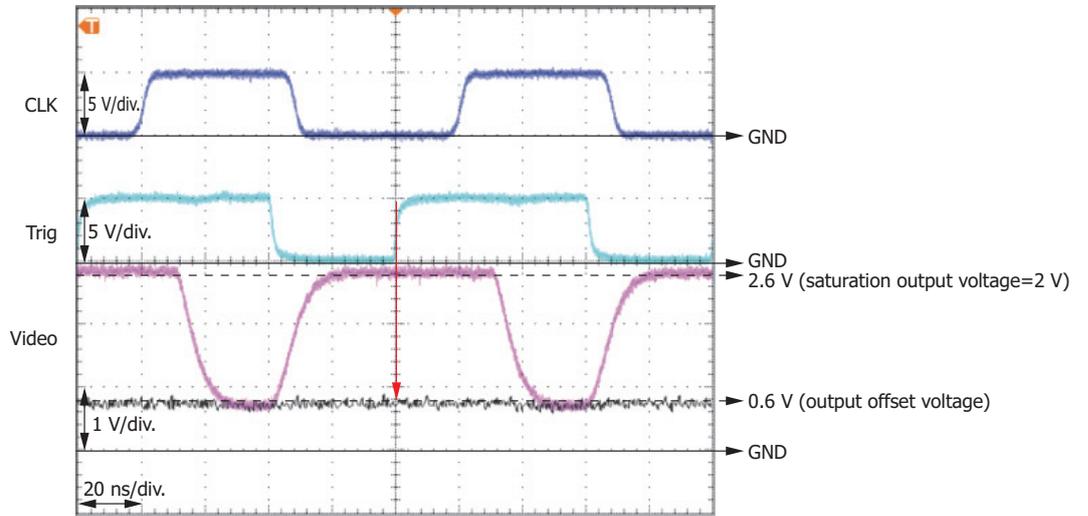


KMPDC0930EA

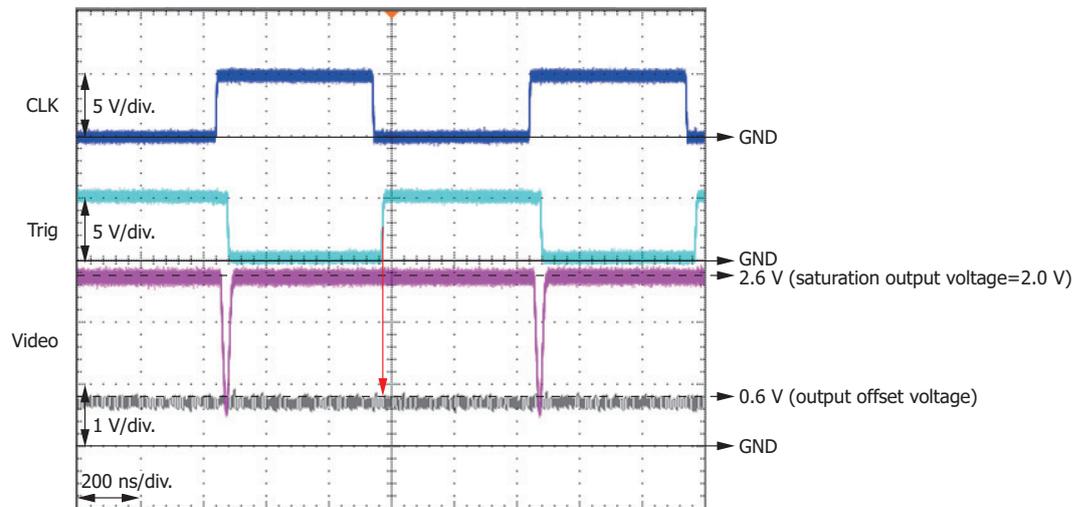
**Output waveform of a pixel**

The timing for acquiring the Video signal is synchronized with the rising edge of a trigger pulse (See red arrow below).

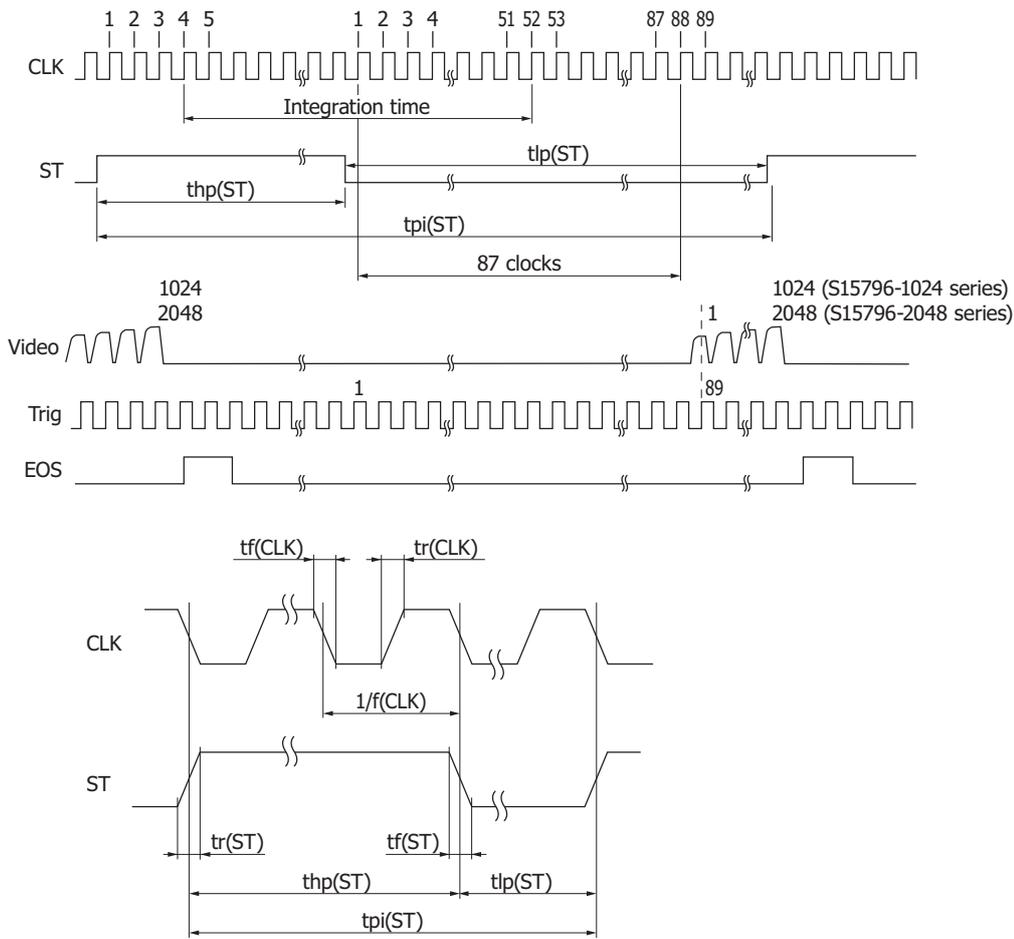
$f(\text{CLK})=\text{DR}=10\text{ MHz}$



$f(\text{CLK})=\text{DR}=1\text{ MHz}$



**Timing chart**



KMPDC0932EA

Parameter	Symbol	Min.	Typ.	Max.	Unit
Start pulse period	tpi(ST)	106/f(CLK)	-	-	s
Start pulse high period*15	thp(ST)	6/f(CLK)	-	-	s
Start pulse low period	tlp(ST)	100/f(CLK)	-	-	s
Start pulse rise/fall times	tr(ST), tf(ST)	0	10	30	ns
Clock pulse duty	-	45	50	55	%
Clock pulse rise/fall times	tr(CLK), tf(CLK)	0	10	30	ns

\*15: The integration time equals the high period of ST plus 48 CLK cycles.

The shift register starts operation at the rising edge of CLK immediately after ST goes low.

The integration time can be changed by changing the ratio of the high and low periods of ST.

If the first Trig pulse after ST goes low is counted as the first pulse, the Video signal is acquired at the rising edge of the 89th Trig pulse.

**❏ Operation examples**

- When outputting from all 1024 pixels (S15796-1024, S15796-1024-20)

When the clock pulse frequency is maximized (data rate is also maximized), the time of one scan is minimized, and the integration time is maximized.

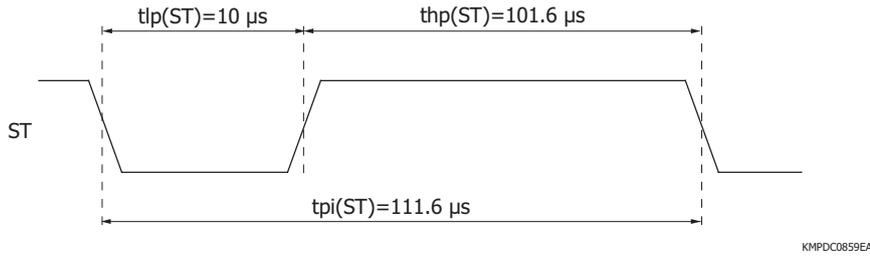
Clock pulse frequency=Data rate=10 MHz

Start pulse cycle =  $1116/f(\text{CLK}) = 1116/10 \text{ MHz} = 111.6 \mu\text{s}$

High period of start pulse = Start pulse cycle - Start pulse's low period min.

$$= 1116/f(\text{CLK}) - 100/f(\text{CLK}) = 1116/10 \text{ MHz} - 100/10 \text{ MHz} = 101.6 \mu\text{s}$$

Integration time is equal to the high period of start pulse + 48 cycles of clock pulses, so it will be  $101.6 + 4.8 = 106.4 \mu\text{s}$ .



- When outputting from all 2048 pixels (S15796-2048, S15796-2048-20)

When the clock pulse frequency is maximized (data rate is also maximized), the time of one scan is minimized, and the integration time is maximized.

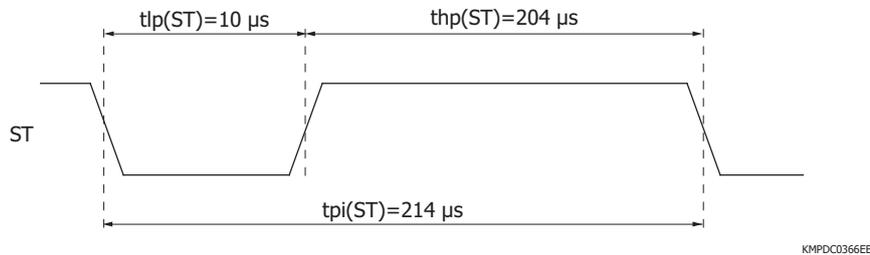
Clock pulse frequency=Data rate=10 MHz

Start pulse cycle =  $2140/f(\text{CLK}) = 2140/10 \text{ MHz} = 214 \mu\text{s}$

High period of start pulse = Start pulse cycle - Start pulse's low period min.

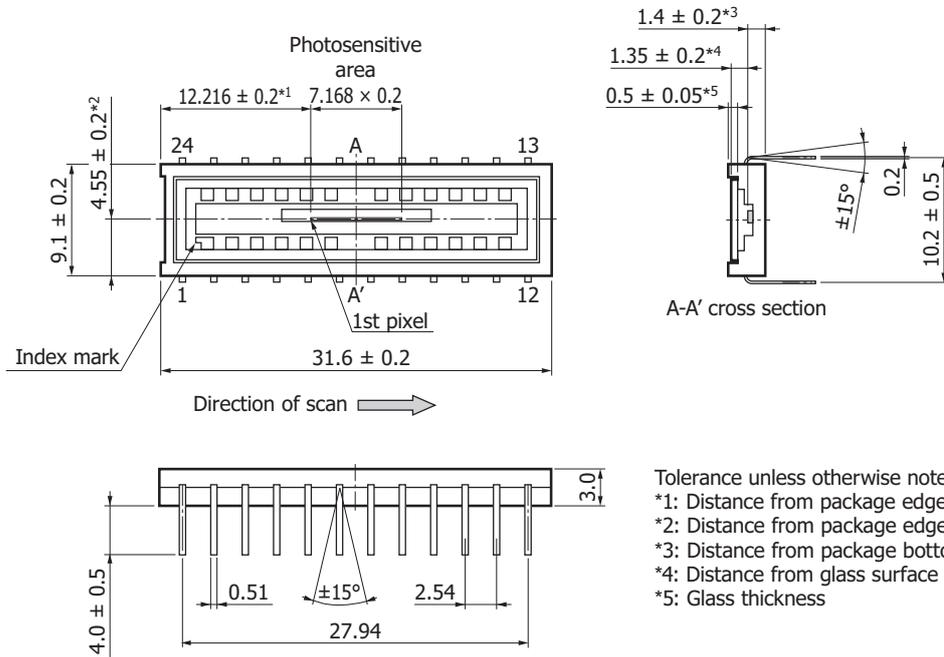
$$= 2140/f(\text{CLK}) - 100/f(\text{CLK}) = 2140/10 \text{ MHz} - 100/10 \text{ MHz} = 204 \mu\text{s}$$

Integration time is equal to the high period of start pulse + 48 cycles of clock pulses, so it will be  $204 + 4.8 = 208.8 \mu\text{s}$ .



**Dimensional outlines (unit: mm)**

S15796-1024



Tolerance unless otherwise noted:  $\pm 0.1$   
 \*1: Distance from package edge to photosensitive area edge  
 \*2: Distance from package edge to photosensitive area center  
 \*3: Distance from package bottom to photosensitive surface  
 \*4: Distance from glass surface to photosensitive surface  
 \*5: Glass thickness

KMPDA0366EA

**Pin connections**

Pin no.	Symbol	I/O	Description	Pin no.	Symbol	I/O	Description
1	NC		No connection	13	NC		No connection
2	NC		No connection	14	NC		No connection
3	Vdd	I	Supply voltage	15	NC		No connection
4	Vss		GND	16	Video	O	Video signal <sup>*16</sup>
5	CLK	I	Clock pulse	17	EOS	O	End of scan
6	NC		No connection	18	NC		No connection
7	NC		No connection	19	NC		No connection
8	Vss		GND	20	Vlcp	O	Bias voltage for negative voltage circuit <sup>*17</sup>
9	Vdd	I	Supply voltage	21	Trig	O	Trigger pulse for video signal capture <sup>*18</sup>
10	NC		No connection	22	ST	I	Start pulse
11	NC		No connection	23	NC		No connection
12	NC		No connection	24	NC		No connection

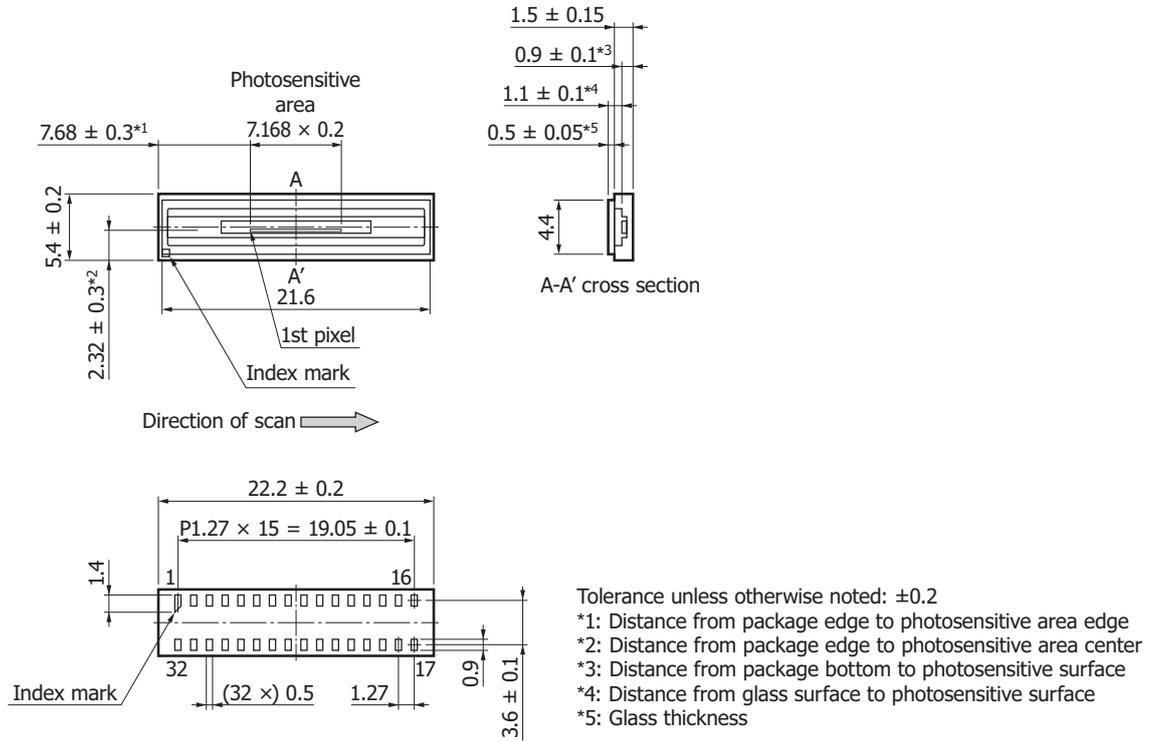
\*16: Connect a buffer amplifier for impedance conversion to the video output terminal so as to minimize the current flow. As the buffer amplifier, use a high input impedance op-amp with JFET or CMOS input.

\*17: Approximately -1.5 V generated by the negative voltage circuit inside the chip is output to the terminal. To maintain the voltage, insert a capacitor around 1  $\mu\text{F}$  between Vlcp and GND.

\*18: We recommend capturing video signal using the trigger pulse output from Trig.

Note: Leave the "NC" terminals open and do not connect them to GND.

S15796-1024-20



KMPDA0367EA

Pin connections

Pin no.	Symbol	I/O	Description	Pin no.	Symbol	I/O	Description
1	NC		No connection	17	NC		No connection
2	NC		No connection	18	NC		No connection
3	NC		No connection	19	NC		No connection
4	NC		No connection	20	NC		No connection
5	Vdd	I	Supply voltage	21	Video	O	Video signal*19
6	Vss		GND	22	NC		No connection
7	CLK	I	Clock pulse	23	EOS	O	End of scan
8	Vss		GND	24	NC		No connection
9	NC		No connection	25	NC		No connection
10	NC		No connection	26	Vlcp	I	Bias voltage for negative voltage circuit*20
11	Vss		GND	27	Trig	O	Trigger pulse for video signal capture*21
12	Vdd	I	Supply voltage	28	ST	I	Start pulse
13	NC		No connection	29	NC		No connection
14	NC		No connection	30	NC		No connection
15	NC		No connection	31	NC		No connection
16	NC		No connection	32	NC		No connection

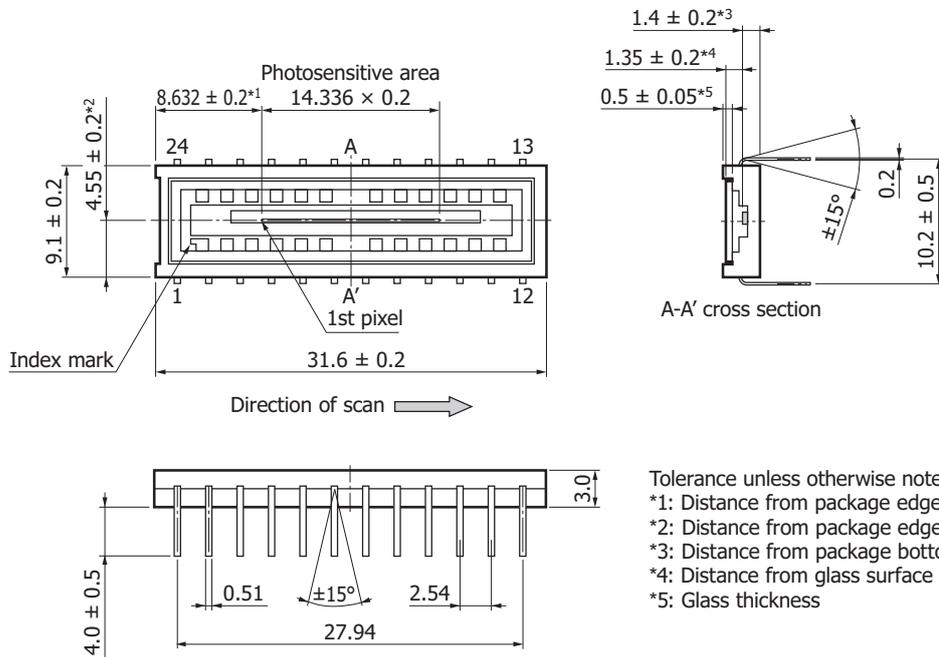
\*19: Connect a buffer amplifier for impedance conversion to the video output terminal so as to minimize the current flow. As the buffer amplifier, use a high input impedance op-amp with JFET or CMOS input.

\*20: Approximately -1.5 V generated by the negative voltage circuit inside the chip is output to the terminal. To maintain the voltage, insert a capacitor around 1  $\mu\text{F}$  between Vlcp and GND.

\*21: We recommend capturing video signal using the trigger pulse output from Trig.

Note: Leave the "NC" terminals open and do not connect them to GND.

S15796-2048



Tolerance unless otherwise noted:  $\pm 0.1$   
 \*1: Distance from package edge to photosensitive area edge  
 \*2: Distance from package edge to photosensitive area center  
 \*3: Distance from package bottom to photosensitive surface  
 \*4: Distance from glass surface to photosensitive surface  
 \*5: Glass thickness

KMPDA0364EA

Pin connections

Pin no.	Symbol	I/O	Description	Pin no.	Symbol	I/O	Description
1	Vdd	I	Supply voltage	13	Video	O	Video signal*22
2	Vss		GND	14	NC		No connection
3	CLK	I	Clock pulse	15	EOS	O	End of scan
4	NC		No connection	16	NC		No connection
5	NC		No connection	17	NC		No connection
6	NC		No connection	18	NC		No connection
7	NC		No connection	19	NC		No connection
8	NC		No connection	20	NC		No connection
9	NC		No connection	21	NC		No connection
10	NC		No connection	22	Vlcp	O	Bias voltage for negative voltage circuit*23
11	Vss		GND	23	Trig	O	Trigger pulse for video signal capture*24
12	Vdd	I	Supply voltage	24	ST	I	Start pulse

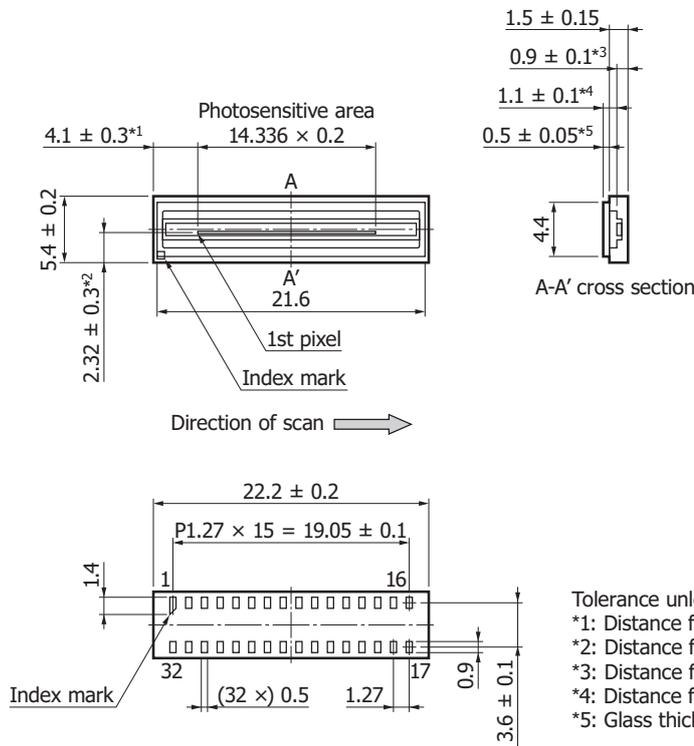
\*22: Connect a buffer amplifier for impedance conversion to the video output terminal so as to minimize the current flow. As the buffer amplifier, use a high input impedance op-amp with JFET or CMOS input.

\*23: Approximately -1.5 V generated by the negative voltage circuit inside the chip is output to the terminal. To maintain the voltage, insert a capacitor around 1  $\mu\text{F}$  between Vlcp and GND.

\*24: We recommend capturing video signal using the trigger pulse output from Trig.

Note: Leave the "NC" terminals open and do not connect them to GND.

S15796-2048-20



KMPDA0365EA

Pin connections

Pin no.	Symbol	I/O	Description	Pin no.	Symbol	I/O	Description
1	Vdd	I	Supply voltage	17	Video	O	Video signal*25
2	Vss		GND	18	NC		No connection
3	CLK	I	Clock pulse	19	EOS	O	End of scan
4	NC		No connection	20	NC		No connection
5	NC		No connection	21	NC		No connection
6	NC		No connection	22	NC		No connection
7	NC		No connection	23	NC		No connection
8	Vss		GND	24	NC		No connection
9	NC		No connection	25	NC		No connection
10	NC		No connection	26	NC		No connection
11	NC		No connection	27	NC		No connection
12	NC		No connection	28	NC		No connection
13	NC		No connection	29	NC		No connection
14	NC		No connection	30	Vlcp	I	Bias voltage for negative voltage circuit*26
15	Vss		GND	31	Trig	O	Trigger pulse for video signal capture*27
16	Vdd	I	Supply voltage	32	ST	I	Start pulse

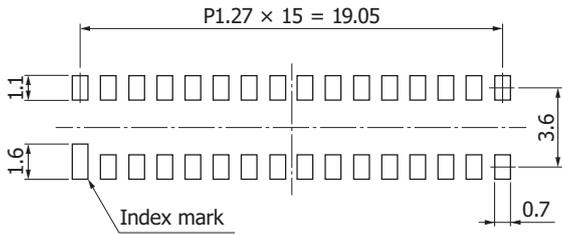
\*25: Connect a buffer amplifier for impedance conversion to the video output terminal so as to minimize the current flow. As the buffer amplifier, use a high input impedance operational amplifier with JFET or CMOS input.

\*26: Approximately -1.5 V generated by the negative voltage circuit inside the chip is output to the terminal. To maintain the voltage, insert a capacitor around 1 μF between Vlcp and GND.

\*27: We recommend capturing video signal using the trigger pulse output from Trig.

Note: Leave the "NC" terminals open and do not connect them to GND.

Recommended land pattern (S15796-1024-20, S15796-2048-20, unit: mm)

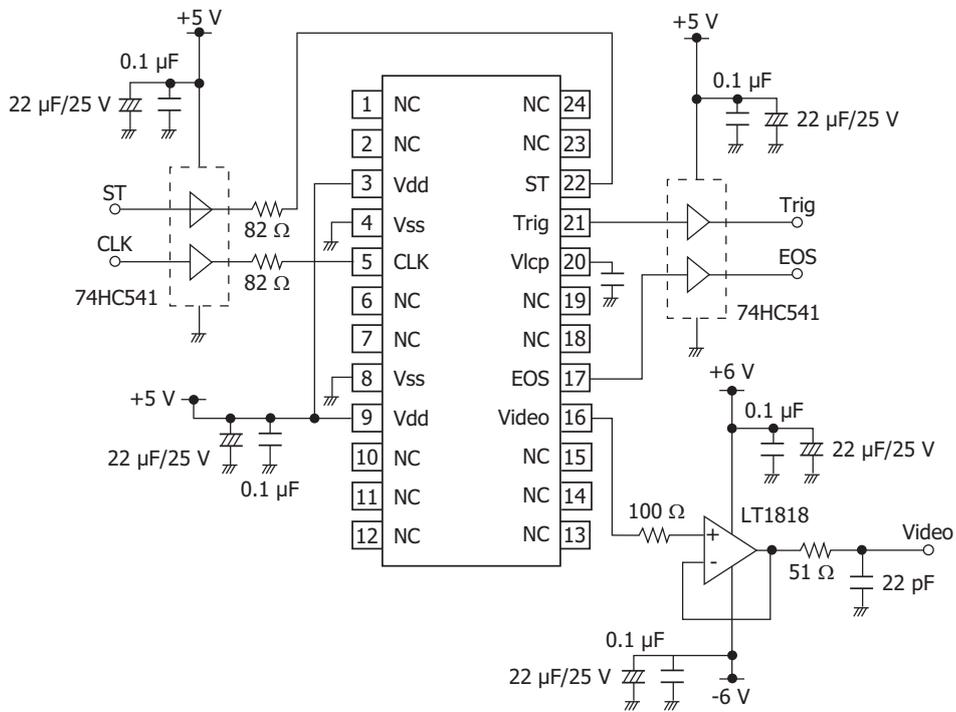


Tolerance unless otherwise noted: ±0.1

KMPDC0944EA

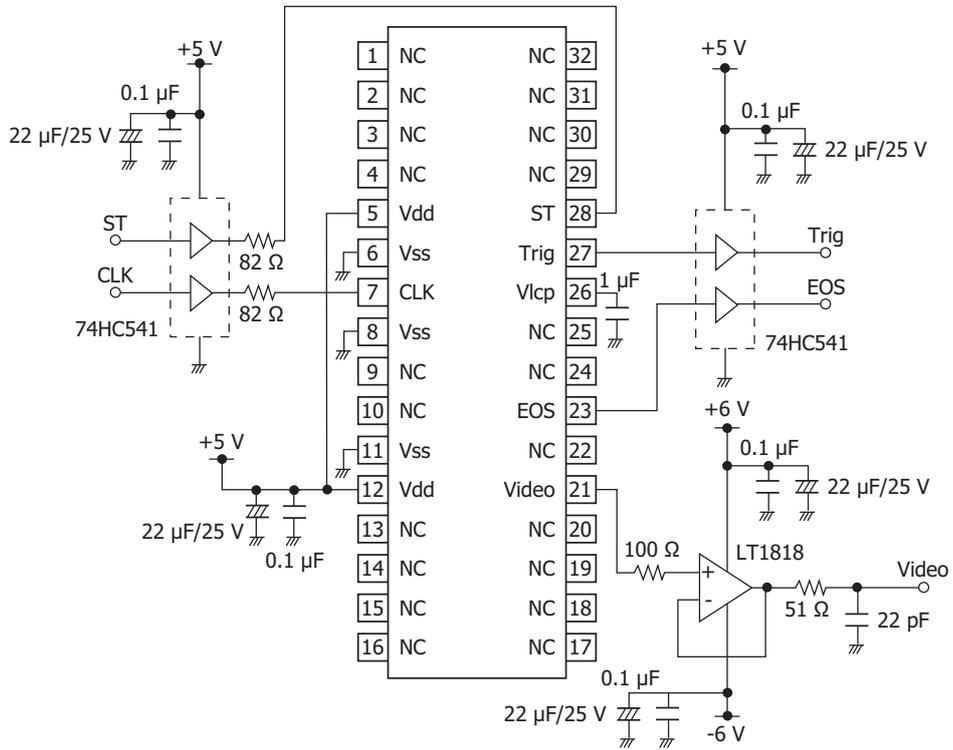
Application circuit examples

S15796-1024



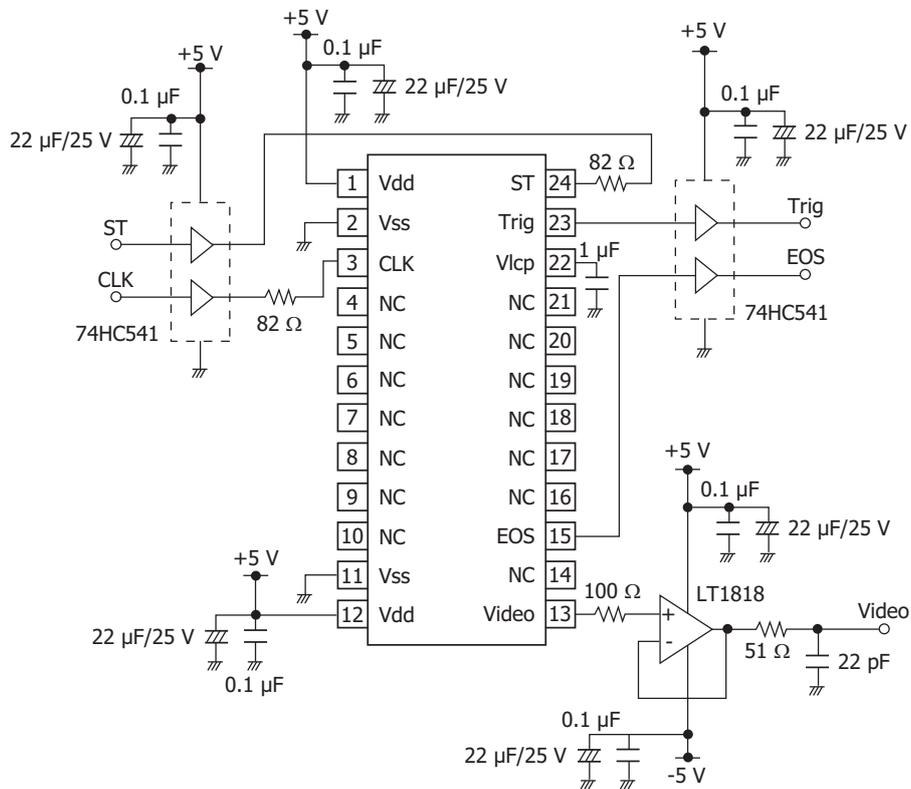
KMPDC0934EA

S15796-1024-20



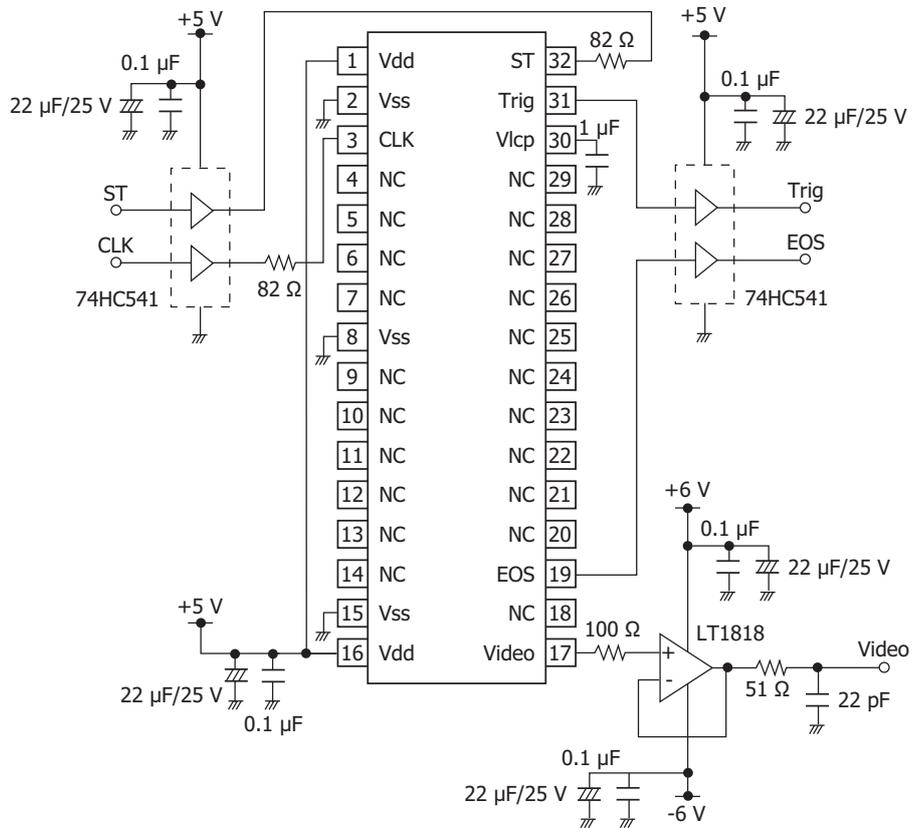
KMPDC0935EA

S15796-2048



KMPDC0564EA

S15796-2048-20



KMPDC0933EA

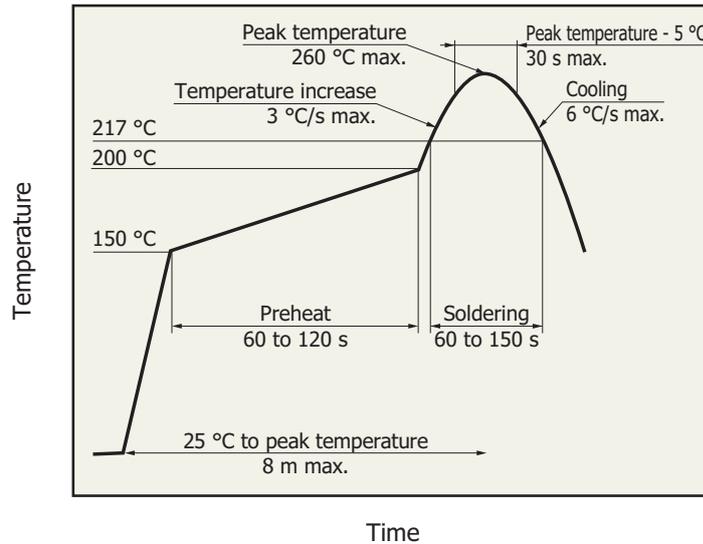
**Recommended soldering conditions**

S15796-1024, S15796-2048

Parameter	Specification	Note
Soldering temperature	260 °C max. (5 seconds or less)	

Note: When you set soldering conditions, check that problems do not occur in the product by testing out the conditions in advance.

S15796-1024-20, S15796-2048-20



KSPDB0419EA

Note:

- This product supports lead-free soldering. After unpacking, store it in an environment at a temperature of 30 °C or less and a humidity of 60% or less, and perform soldering within 1 month.
- The effect that the product receives during reflow soldering varies depending on the circuit board and reflow oven that are used. When you set reflow soldering conditions, check that problems do not occur in the product by testing out the conditions in advance.
- Drastic changes in temperature can cause problems. Keep the temperature change to less than 3 °C/second for heating and to less than 6 °C/second for cooling. Note that the bonding portion between the ceramic base and the glass may discolor after reflow soldering, but this has no adverse effects on the hermetic sealing of the product.

## ⚠ Precautions

### (1) Electrostatic countermeasures

These devices has a built-in protection circuit against static electrical charges. However, to prevent destroying the devices with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges. Also protect these devices from surge voltages which might be caused by peripheral equipment.

### (2) Light input window

If dust or stain adheres to the surface of the input window glass, it will appear as black spots on the image. When cleaning, avoid rubbing the window surface with dry cloth, dry cotton swab or the like, since doing so may generate static electricity. Use soft cloth, paper, a cotton swab, or the like moistened with alcohol to wipe off dust and stain. Then blow compressed air so that no stain remains.

### (3) UV light irradiation

These products are designed to reduce characteristic deterioration under UV light irradiation, but unnecessary irradiation should be avoided. Also avoid exposing the bonding sections of the glass to UV light.

## ⚠ Related information

[www.hamamatsu.com/sp/ssd/doc\\_en.html](http://www.hamamatsu.com/sp/ssd/doc_en.html)

### ■ Precautions

- Disclaimer
- Image sensors
- Surface mount type products

### ■ Technical information

- CMOS linear image sensors

Information described in this material is current as of November 2021.

Product specifications are subject to change without prior notice due to improvements or other reasons. This document has been carefully prepared and the information contained is believed to be accurate. In rare cases, however, there may be inaccuracies such as text errors. Before using these products, always contact us for the delivery specification sheet to check the latest specifications.

The product warranty is valid for one year after delivery and is limited to product repair or replacement for defects discovered and reported to us within that one year period. However, even if within the warranty period we accept absolutely no liability for any loss caused by natural disasters or improper product use. Copying or reprinting the contents described in this material in whole or in part is prohibited without our prior permission.

# HAMAMATSU

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