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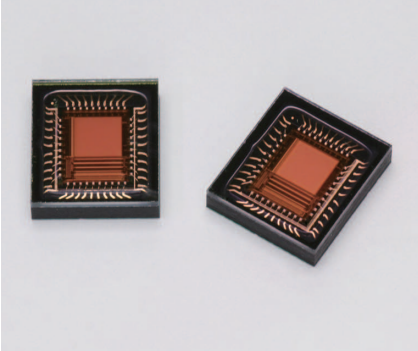
# Distance area image sensor



S11962-01CR

## Measures the distance to an object by TOF (Time-Of-Flight) method

The distance image sensors are designed to measure the distance to an object by TOF method. When used in combination with a pulse modulated light source, this sensor outputs phase difference information on the timing that the light is emitted and received. The sensor output signals are arithmetically processed by an external signal processing circuit or a PC to obtain distance data.

### Features

- **High-speed charge transfer structure**
- **Operates with minimal detection errors even under fluctuating (charge drain function)**
- **Real-time distance measurement**

### Applications

- **Obstacle detection (self-driving, robots, etc.)**
- **Security (intrusion detection, etc.)**
- **Shape recognition (logistics, robots, etc.)**
- **Motion capture**

### Structure

| Parameter | Specification | Unit |
|---|---|---|
| Image size | 2.56 × 2.56 | mm |
| Pixel size | 40 × 40 | µm |
| Pixel pitch | 40 | µm |
| Number of pixels | 72 × 72 | pixels |
| Number of effective pixels | 64 × 64 | pixels |
| Package | 48-pin PWB | - |
| Window material | AR-coated glass | - |

Note: This product is not hermetically sealed.

### Absolute maximum ratings

| Parameter | | Symbol | Condition | Value | Unit |
|---|---|---|---|---|---|
| Analog supply voltage | | Vdd(A) | Ta=25 °C | -0.3 to +6 | V |
| Digital supply voltage | | Vdd(D) | Ta=25 °C | -0.3 to +6 | V |
| Analog input terminal voltage | Pixel amplifier | Vsf | Ta=25 °C | -0.3 to Vdd(A) + 0.3 | V |
| | Pixel reset | Vr | | | |
| | Output offset | Vref | | | |
| | Photosensitive area | Vpg | | | |
| Digital input terminal voltage | Frame reset pulse | reset | Ta=25 °C | -0.3 to Vdd(D) + 0.3 | V |
| | Frame synchronous trigger pulse | vst | | | |
| | Line synchronous trigger pulse | hst | | | |
| | Pixel reset pulse | ext_res | | | |
| | Master clock pulse | mclk | | | |
| Charge transfer clock pulse voltage | | VTX1, VTX2, VTX3 | Ta=25 °C | -0.3 to Vdd(A) + 0.3 | V |
| Operating temperature | | Topr | No dew condensation*1 | -25 to +85 | °C |
| Storage temperature | | Tstg | No dew condensation*1 | -40 to +100 | °C |
| Reflow soldering conditions*2 | | Tsol | | 260 °C max. 2 times (see P.10) | - |

*1: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.
*2: JEDEC level 3
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

## Recommended terminal voltage (Ta=25 °C)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Analog supply voltage | | Vdd(A) | 4.75 | 5 | 5.25 | V |
| Digital supply voltage | | Vdd(D) | 4.75 | 5 | 5.25 | V |
| Bias voltage | Pixel amplifier | Vsf | 4.5 | 5 | Vdd(A) | V |
| | Pixel reset | Vr | 3.7 | 3.9 | 4.1 | V |
| | Output offset | Vref | 2.3 | 2.5 | 2.7 | V |
| | Photosensitive area | Vpg | 0.8 | 1.0 | 1.2 | V |
| Frame reset pulse voltage | High level | reset | Vdd(D) × 0.8 | - | - | V |
| | Low level | | - | - | Vdd(D) × 0.2 | |
| Frame synchronous trigger pulse voltage | High level | vst | Vdd(D) × 0.8 | - | - | V |
| | Low level | | - | - | Vdd(D) × 0.2 | |
| Line synchronous trigger pulse voltage | High level | hst | Vdd(D) × 0.8 | - | - | V |
| | Low level | | - | - | Vdd(D) × 0.2 | |
| Master clock pulse voltage | High level | mclk | Vdd(D) × 0.8 | - | - | V |
| | Low level | | - | - | Vdd(D) × 0.2 | |
| Pixel reset pulse voltage | High level | ext_res | Vdd(D) × 0.8 | - | - | V |
| | Low level | | - | - | Vdd(D) × 0.2 | |
| Output signal effective period pulse voltage | High level | oe | Vdd(D) × 0.8 | - | - | V |
| | Low level | | - | - | Vdd(D) × 0.2 | |
| Output signal synchronous pulse voltage | High level | dclk | Vdd(D) × 0.8 | - | - | V |
| | Low level | | - | - | Vdd(D) × 0.2 | |
| Non-readout period pulse voltage | High level | dis_read | Vdd(D) × 0.8 | - | - | V |
| | Low level | | - | - | Vdd(D) × 0.2 | |

## Electrical characteristics [Ta=25 °C, Vdd(A)=Vdd(D)=5 V]

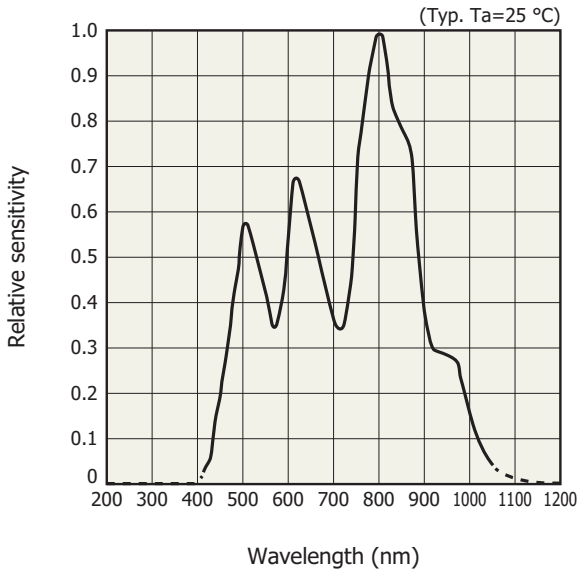
| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Clock pulse frequency | f(mclk) | | 1 M | - | 10 M | Hz |
| Video data rate | VR | | - | f(mclk) | - | Hz |
| Current consumption | Ic | Dark state | - | 10 | 20 | mA |

## Electrical and optical characteristics [Ta=25 °C, Vdd(A)=Vdd(D)=5 V, Vsf=5 V, Vr=4.25 V, MCLK=5 MHz]

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Spectral response range | λ | 400 to 1100 | | | nm |
| Peak sensitivity wavelength | λp | - | 800 | - | nm |
| Photosensitivity*3 | S | $1.15 \times 10^{12}$ | $2.3 \times 10^{12}$ | $4.6 \times 10^{12}$ | V/W·s |
| Dark output | Vd | - | 0.5 | 10 | V/s |
| Random noise | RN | - | 0.8 | 1.6 | mV rms |
| Dark output voltage*4 | Vor | Vref + 1.0 | - | Vref + 2.1 | V |
| Saturation output voltage | Vsat | Vref - 1.1 | - | Vref + 0.3 | V |
| Sensitivity ratio*5 | SR | 0.7 | - | 1.43 | - |
| Photoresponse nonuniformity*6 | PRNU | - | - | ±10 | % |

*3: Monochromatic wavelength source (λ=805 nm)
*4: Output voltage right after reset in dark state
*5: Sensitivity ratio of Vout1 (VTX1=3 V, VTX2=VTX3=0 V) to Vout2 (VTX2=3 V, VTX1=VTX3=0 V)
*6: Photoresponse nonuniformity (PRNU) is the output nonuniformity that occurs when the entire photosensitive area is uniformly illuminated by white light which is approx. 50% of the saturation level. PRNU is measured using the pixels excluding the pixels of the 4 outermost lines and defective pixels, and is defined as follows:
PRNU= ΔX/X × 100 (%)
X: average output of all pixels, ΔX: standard deviation of pixel output

## Spectral response

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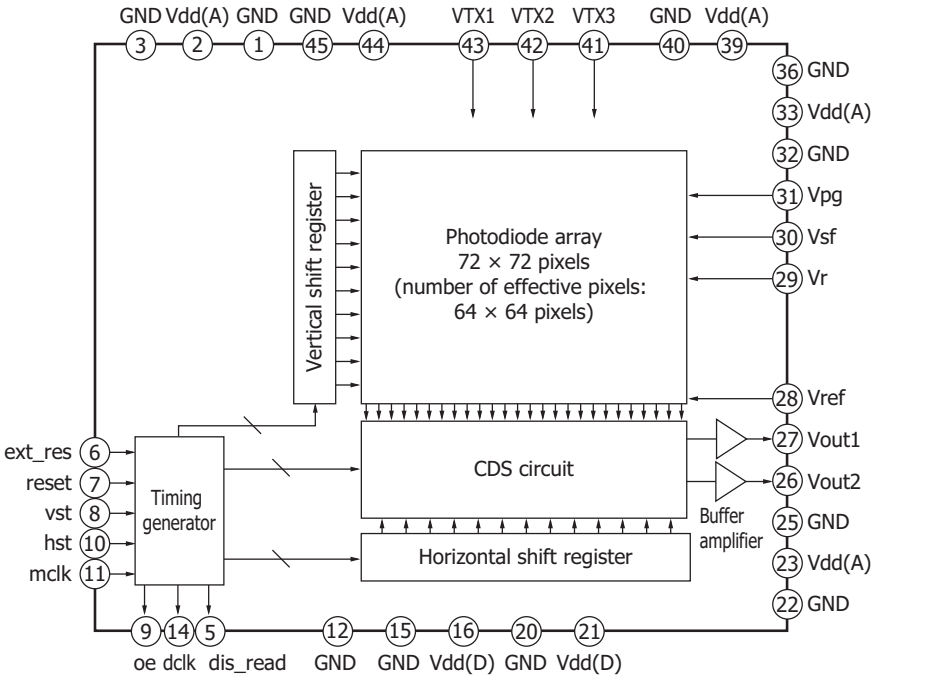
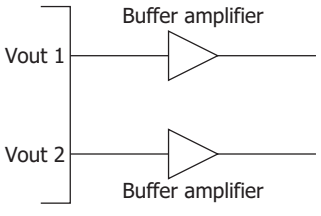
## Block diagram




KMPDC0438EC

## Basic connection example

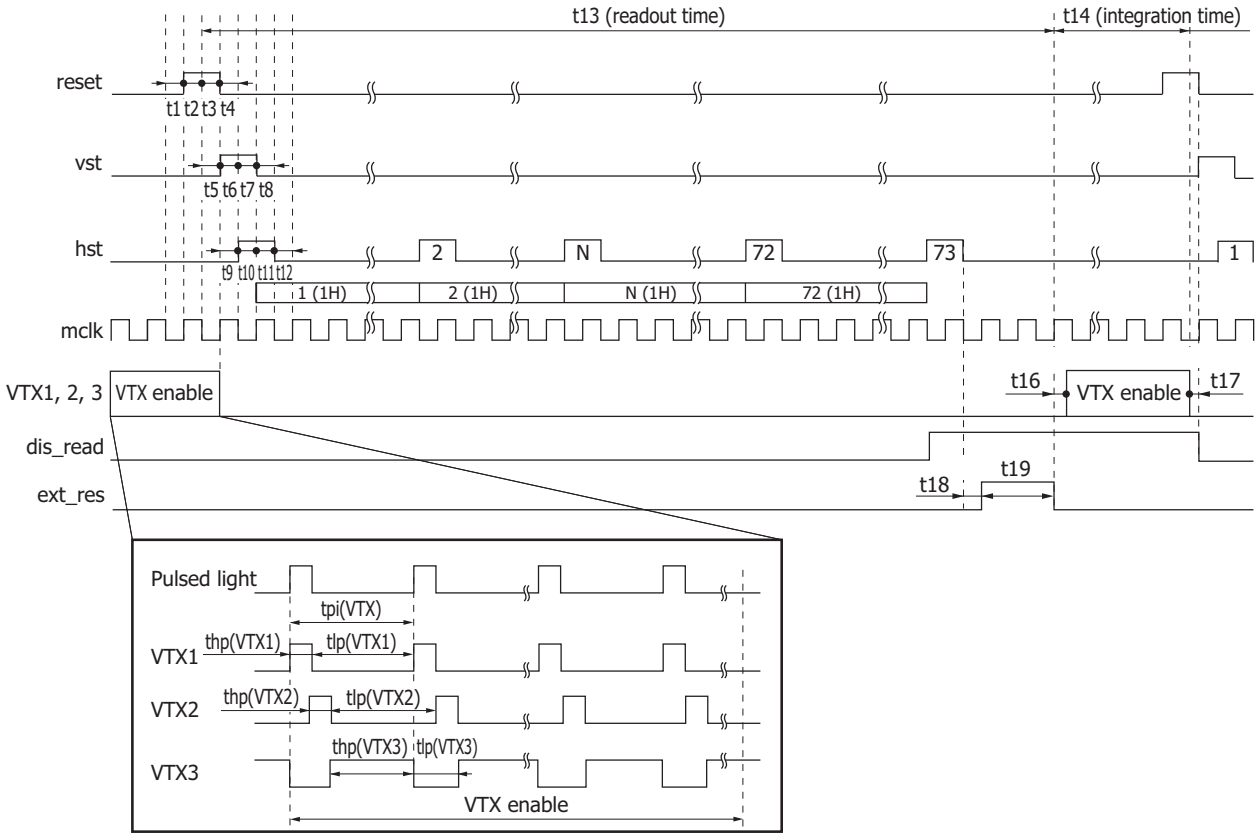



KMPDC0486EA

## Timing chart

Using VTX3 allows changing the light source duty ratio to increase the light emission power. When thp(VTX3) is set to 0 ns, the light source can be driven with a duty ratio of 50%.

■ Frame timing

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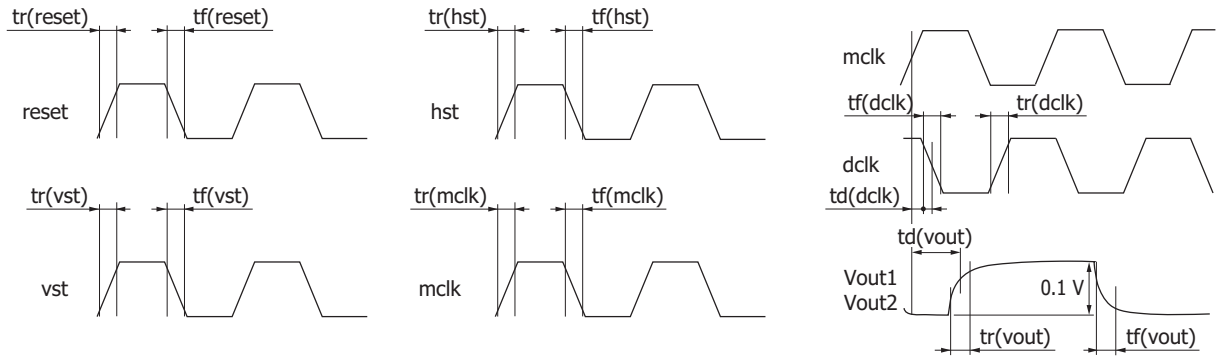
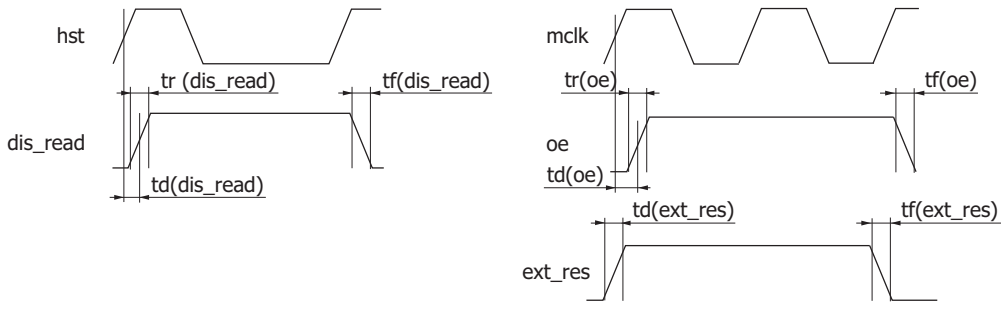



KMPDC0440EA

## Calculation method of frame rate

Frame rate=1/(Time per frame)
=1/(Integration time + Readout time)

Integration time:
It is necessary to be changed by the required distance accuracy and usage environment factors such as fluctuating background light.

$$\text{Readout time}=\frac{1}{\text{Clock pulse frequency}} \times \text{Horizontal timing clock} \times \text{Number of vertical pixels}$$

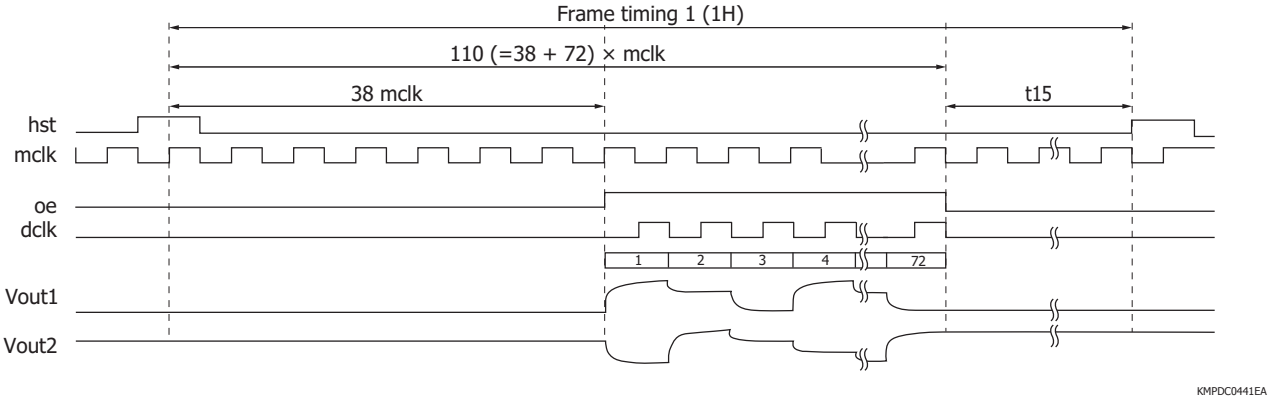
=Time per clock (Readout time per pixel) × Horizontal timing clocks × Number of vertical pixels

Calculation example of readout time (clock pulse frequency: 5 MHz, horizontal timing clocks: 110, number of vertical pixels: 72)

$$\text{Readout time}=\frac{1}{5 \times 10^6\ [\text{Hz}]} \times 110 \times 72$$

=200 [ns] × 110 × 72
=1.584 [ms]

■ Horizontal timing



| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Master clock pulse duty ratio | - | 45 | 50 | 55 | % |
| Master clock pulse rise and fall times | tr(mclk), tf(mclk) | 0 | - | 20 | ns |
| Frame reset pulse rise and fall times | tr(reset), tf(reset) | 0 | - | 20 | ns |
| Frame synchronous trigger pulse rise and fall times | tr(vst), tf(vst) | 0 | - | 20 | ns |
| Line synchronous trigger pulse rise and fall times | tr(hst), tf(hst) | 0 | - | 20 | ns |
| Pixel reset pulse rise and fall times | tr(ext_res), tf(ext_res) | 0 | - | 20 | ns |
| Time from falling edge of master clock pulse to rising edge of frame reset pulse | t1 | 1/4 × 1/f(mclk) | - | 1/2 × 1/f(mclk) | s |
| Time from rising edge of frame reset pulse to falling edge of master clock pulse | t2 | 1/4 × 1/f(mclk) | - | 1/2 × 1/f(mclk) | s |
| Time from falling edge of master clock pulse to falling edge of frame reset pulse | t3 | 1/4 × 1/f(mclk) | - | 1/2 × 1/f(mclk) | s |
| Time from falling edge of frame reset pulse to falling edge of master clock pulse | t4 | 1/4 × 1/f(mclk) | - | 1/2 × 1/f(mclk) | s |
| Time from falling edge of master clock pulse to rising edge of frame synchronous trigger pulse | t5 | 1/4 × 1/f(mclk) | - | 1/2 × 1/f(mclk) | s |
| Time from rising edge of frame synchronous trigger pulse to falling edge of master clock pulse | t6 | 1/4 × 1/f(mclk) | - | 1/2 × 1/f(mclk) | s |
| Time from falling edge of master clock pulse to falling edge of frame synchronous trigger pulse | t7 | 1/4 × 1/f(mclk) | - | 1/2 × 1/f(mclk) | s |
| Time from falling edge of frame synchronous trigger pulse to falling edge of master clock pulse | t8 | 1/4 × 1/f(mclk) | - | 1/2 × 1/f(mclk) | s |
| Time from rising edge of master clock pulse to rising edge of line synchronous trigger pulse | t9 | 1/4 × 1/f(mclk) | - | 1/2 × 1/f(mclk) | s |
| Time from rising edge of line synchronous trigger pulse to rising edge of master clock pulse | t10 | 1/4 × 1/f(mclk) | - | 1/2 × 1/f(mclk) | s |
| Time from rising edge of master clock pulse to falling edge of line synchronous trigger pulse | t11 | 1/4 × 1/f(mclk) | - | 1/2 × 1/f(mclk) | s |
| Time from falling edge of line synchronous trigger pulse to rising edge of master clock pulse | t12 | 1/4 × 1/f(mclk) | - | 1/2 × 1/f(mclk) | s |
| Readout time | t13 | (110/f(mclk) + t15) x 72 + t18 + t19 | - | - | s |
| Integration time | t14 | - | 10 | - | ms |
| Time from rising edge of master clock pulse (after reading signals from all pixels) to rising edge of master clock pulse (hst: high period) | t15 | 10/f(mclk) | - | - | s |
| Time from falling edge of master clock pulse to rising edge of output signal synchronous pulse | td(dclk) | 0 | 25 | 50 | ns |
| Output signal synchronous pulse output voltage rise time (10 to 90%)*7 | tr(dclk) | - | 20 | 40 | ns |
| Output signal synchronous pulse output voltage fall time (10 to 90%)*7 | tf(dclk) | - | 20 | 40 | ns |
| Time from rising edge of master clock pulse to rising edge of output signal effective period pulse | td(oe) | 0 | 25 | 50 | ns |
| Output signal effective period pulse rise time (10 to 90%)*7 | tr(oe) | - | 20 | 40 | ns |
| Output signal effective period pulse fall time (10 to 90%)*7 | tf(oe) | - | 20 | 40 | ns |
| Settling time of output signal 1, 2 (10 to 90%)*7 *8 | tr(Vout), tf(Vout) | - | 35 | 70 | ns |
| Time from rising edge of master clock pulse to output signal 1, 2 (output 50%)*7 | td(Vout) | - | 40 | 80 | ns |

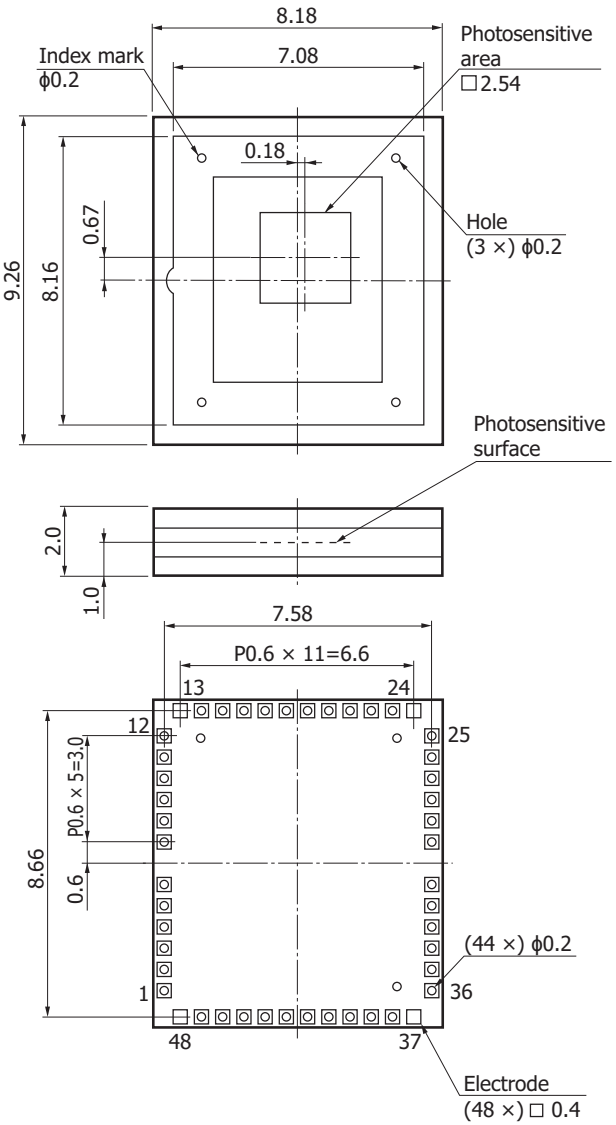
*7: $C_L$=3 pF
*8: Output voltage=0.1 V

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Charge transfer clock pulse interval | | tpi(VTX) | 60 | - | - | ns |
| Charge transfer clock pulse (VTX1) high period | | thp(VTX1) | 30 | - | - | ns |
| Charge transfer clock pulse (VTX1) low period | | tlp(VTX1) | - | tpi(VTX) - thp(VTX2) - thp(VTX3) | - | ns |
| Charge transfer clock pulse (VTX2) high period | | thp(VTX2) | 30 | - | - | ns |
| Charge transfer clock pulse (VTX2) low period | | tlp(VTX2) | - | tpi(VTX) - thp(VTX1) - thp(VTX3) | - | ns |
| Charge transfer clock pulse (VTX3) high period | | thp(VTX3) | 0 | - | - | ns |
| Charge transfer clock pulse (VTX3) low period | | tlp(VTX3) | - | tpi(VTX) - thp(VTX1) - thp(VTX2) | - | ns |
| Charge transfer clock pulse voltage rise time | | tr(VTX) | - | 3 | - | ns |
| Charge transfer clock pulse voltage fall time | | tf(VTX) | - | 3 | - | ns |
| Charge transfer clock pulse voltage | High level | VTX1, VTX2, VTX3 | - | 3 | - | V |
| | Low level | | - | 0 | - | |
| Time from falling edge of pixel reset pulse to "VTX enable period=on" | | t16 | 0 | - | - | s |
| Time from "VTX enable period=off" to falling edge of frame reset pulse | | t17 | 0 | - | - | s |
| Time from rising edge of line synchronous trigger pulse (last pulse) to rising edge of pixel reset pulse | | t18 | 0 | - | - | s |
| Pixel reset pulse high period | | t19 | 10 | - | - | µs |
| Time from rising edge of line synchronous trigger pulse to rising edge of non-readout period pulse*7 | | td(dis_read) | - | 25 | 50 | ns |
| Non-readout period pulse rise time (10 to 90%)*7 | | tr(dis_read) | - | 20 | 40 | ns |
| Non-readout period pulse fall time (10 to 90%)*7 | | tf(dis_read) | - | 20 | 40 | ns |

## Input terminal capacitance (Ta=25 °C, Vdd=5 V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Charge transfer clock pulse internal load capacitance | $C_{LTX}$ | - | 100 | - | pF |

## Dimensional outline (unit: mm)




Tolerance unless otherwise noted: ±0.2, ±2°

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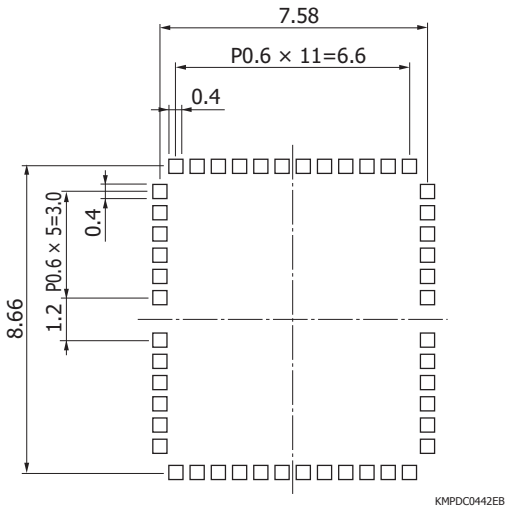
## Recommended land pattern (unit: mm)



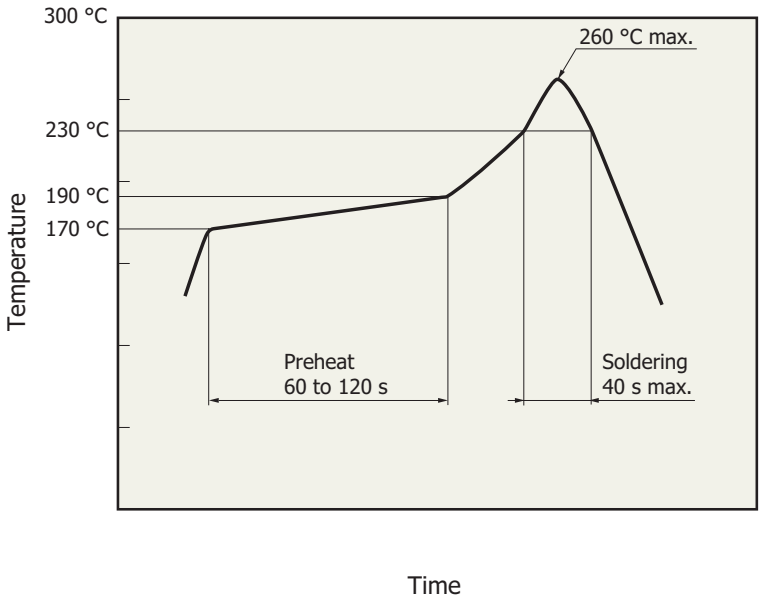

KMPDC0442EB

## Pin connections

| Pin no. | Symbol | I/O | Description |
|---|---|---|---|
| 1 | GND | I | Ground |
| 2 | Vdd(A) | I | Analog supply voltage |
| 3 | GND | I | Ground |
| 4 | NC | - | No connection |
| 5 | dis_read | O | Non-readout period pulse |
| 6 | ext_res | I | Pixel reset pulse |
| 7 | reset | I | Frame reset pulse |
| 8 | vst | I | Frame synchronous trigger pulse |
| 9 | oe | O | Output signal effective period pulse |
| 10 | hst | I | Line synchronous trigger pulse |
| 11 | mclk | I | Master clock pulse |
| 12 | GND | I | Ground |
| 13 | NC | - | No connection |
| 14 | dclk | O | Output signal synchronous pulse |
| 15 | GND | I | Ground |
| 16 | Vdd(D) | I | Digital supply voltage |
| 17 | NC | - | No connection |
| 18 | NC | - | No connection |
| 19 | NC | - | No connection |
| 20 | GND | I | Ground |
| 21 | Vdd(D) | I | Digital supply voltage |
| 22 | GND | I | Ground |
| 23 | Vdd(A) | I | Analog supply voltage |
| 24 | NC | - | No connection |
| 25 | GND | I | Ground |
| 26 | Vout2 | O | Output signal 2 |
| 27 | Vout1 | O | Output signal 1 |
| 28 | Vref | I | Bias voltage (output offset) |
| 29 | Vr | I | Bias voltage (pixel reset) |
| 30 | Vsf | I | Bias voltage (pixel amplifier) |
| 31 | Vpg | I | Bias voltage (photosensitive area) |
| 32 | GND | I | Ground |
| 33 | Vdd(A) | I | Analog supply voltage |
| 34 | NC | - | No connection |
| 35 | NC | - | No connection |
| 36 | GND | I | Ground |
| 37 | NC | - | No connection |
| 38 | NC | - | No connection |
| 39 | Vdd(A) | I | Analog supply voltage |
| 40 | GND | I | Ground |
| 41 | VTX3 | I | Charge transfer clock pulse 3 |
| 42 | VTX2 | I | Charge transfer clock pulse 2 |
| 43 | VTX1 | I | Charge transfer clock pulse 1 |
| 44 | Vdd(A) | I | Analog supply voltage |
| 45 | GND | I | Ground |
| 46 | NC | - | No connection |
| 47 | NC | - | No connection |
| 48 | NC | - | No connection |

Note: Leave the "NC" terminals open and do not connect them to GND.
Connect impedance convering buffer amplifiers to Vout1/Vout2 so as to minimize the current flow.

## Measured example of temperature profile with hot-air reflow oven for product testing




- This product supports lead-free soldering. After unpacking, store it in an environment at a temperature of 30 °C or less and a humidity of 60% or less, and perform soldering within 168 hours.
- The effect that the product receives during reflow soldering varies depending on the circuit board and reflow oven that are used. Before actual reflow soldering, check for any problems by testing out the reflow soldering methods in advance.

## Related information

www.hamamatsu.com/sp/ssd/doc_en.html

Precautions

- Dislaimer
- Surface mount type products
- Image sensors



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