

NMOS linear image sensor

S3902/S3903 series



**Current output, high UV sensitivity,
excellent linearity, low power consumption**

NMOS linear image sensors are self-scanning photodiode arrays designed specifically as detectors for multichannel spectroscopy. The scanning circuit is made up of N-channel MOS transistors, operates at low power consumption and is easy to handle. Each photodiode has a large active area, high UV sensitivity yet very low noise, delivering a high S/N even at low light levels. NMOS linear image sensors also offer excellent output linearity and wide dynamic range.

The photodiodes of S3902 series have a height of 0.5 mm and are arrayed in a row at a spacing of 50 μm . The photodiodes of S3903 series also have a height of 0.5 mm but are arrayed at a spacing of 25 μm . The photodiodes are available in 3 different pixel quantities for each series: 128 (S3902-128Q), 256 (S3902-256Q, S3903-256Q), 512 (S3902-512Q, S3903-512Q) and 1024 (S3903-1024Q). Quartz glass is the standard window material.

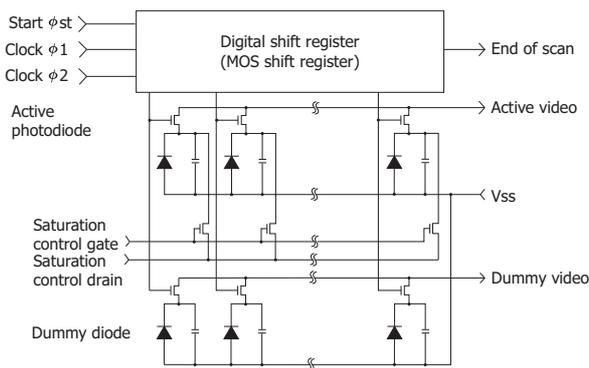
Features

- **Wide active area**
Pixel pitch: 50 μm (S3902 series)
25 μm (S3903 series)
Pixel height: 0.5 mm
- **High UV sensitivity with good stability**
- **Low dark current and high saturation charge allow a long integration time and a wide dynamic range at room temperature**
- **Excellent output linearity and sensitivity spatial uniformity**
- **Lower power consumption: 1 mW max.**
- **Start pulse and clock pulses are CMOS logic compatible**

Applications

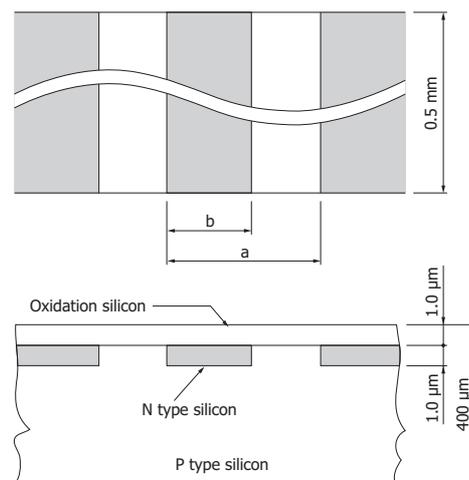
- **Multichannel spectrophotometry**
- **Image readout system**

Equivalent circuit



KMPDC0020EA

Active area structure



S3902 series: a=50 μm , b=45 μm
S3903 series: a=25 μm , b=20 μm

KMPDA0107EA

▣ Absolute maximum ratings

Parameter	Symbol	Value	Unit
Input pulse (ϕ_1 , ϕ_2 , ϕ_{st}) voltage	$V\phi$	15	V
Power consumption*1	P	1	mW
Operating temperature*2	Topr	-40 to +65	°C
Storage temperature	Tstg	-40 to +85	°C

*1: $V\phi=5.0$ V

*2: No condensation

▣ Shape specifications

Parameter	S3902-128Q	S3902-256Q	S3902-512Q	S3903-256Q	S3903-512Q	S3903-1024Q	Unit
Number of pixels	128	256	512	256	512	1024	-
Package length	31.75		40.6	31.75		40.6	mm
Number of pin	22			22			-
Window material	Quartz			Quartz			-
Weight	3.0		3.5	3.0		3.5	g

▣ Specifications (Ta=25 °C)

Parameter	Symbol	S3902 series			S3903 series			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Pixel pitch	-	-	50	-	-	25	-	μm
Pixel height	-	-	0.5	-	-	0.5	-	mm
Spectral response range (10% of peak)	λ	200 to 1000			200 to 1000			nm
Peak sensitivity wavelength	λ_p	-	600	-	-	600	-	nm
Photodiode dark current*3	I_D	-	0.08	0.15	-	0.04	0.08	pA
Photodiode capacitance*3	C_{ph}	-	4	-	-	2	-	pF
Saturation exposure*3 *4	E_{sat}	-	180	-	-	180	-	$\text{m}/\text{x} \cdot \text{s}$
Saturation output charge*3	Q_{sat}	-	10	-	-	5	-	pC
Photo response non-uniformity*5	PRNU	-	-	± 3	-	-	± 3	%

*3: $V_b=2.0$ V, $V\phi=5.0$ V

*4: 2856 K, tungsten lamp

*5: 50% of saturation, excluding the start pixel and last pixel

Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Condition	S3902 series			S3903 series			Unit	
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Clock pulse (φ1, φ2) voltage	High	Vφ1, Vφ2 (H)	-	4.5	5	10	4.5	5	10	V
	Low	Vφ1, Vφ2 (L)	-	0	-	0.4	0	-	0.4	V
Start pulse (φst) voltage	High	Vφst (H)	-	4.5	Vφ1	10	4.5	Vφ1	10	V
	Low	Vφst (L)	-	0	-	0.4	0	-	0.4	V
Video bias voltage*6	Vb	-	1.5	Vφ - 3.0	Vφ - 2.5	1.5	Vφ - 3.0	Vφ - 2.5	V	
Saturation control gate voltage	Vscg	-	-	0	-	-	0	-	V	
Saturation control drain voltage	Vscd	-	-	Vb	-	-	Vb	-	V	
Clock pulse (φ1, φ2) rise / fall time*7	trφ1, trφ2 tfφ1, tfφ2	-	-	20	-	-	20	-	ns	
Clock pulse (φ1, φ2) pulse width	tpwφ1, tpwφ2	-	200	-	-	200	-	-	ns	
Start pulse (φst) rise / fall time	trφst, tfφst	-	-	20	-	-	20	-	ns	
Start pulse (φst) pulse width	tpwφst	-	200	-	-	200	-	-	ns	
Start pulse (φst) and clock pulse (φ2) overlap	tφov	-	200	-	-	200	-	-	ns	
Clock pulse space*7	X1, X2	-	trf - 20	-	-	trf - 20	-	-	ns	
Data rate*8	f	-	0.1	-	2000	0.1	-	2000	kHz	
Video delay time	tvd	50% of saturation *8 *9	-	70 (-128 Q)	-	-	80 (-256 Q)	-	ns	
			-	110 (-256 Q)	-	-	120 (-512 Q)	-	ns	
			-	140 (-512 Q)	-	-	160 (-1024 Q)	-	ns	
Clock pulse (φ1, φ2) line capacitance	Cφ	5 V bias	-	21 (-128 Q)	-	-	27 (-256 Q)	-	pF	
			-	36 (-256 Q)	-	-	50 (-512 Q)	-	pF	
			-	67 (-512 Q)	-	-	100 (-1024 Q)	-	pF	
Saturation control gate (Vscg) line capacitance	Cscg	5 V bias	-	12 (-128 Q)	-	-	12 (-256 Q)	-	pF	
			-	20 (-256 Q)	-	-	24 (-512 Q)	-	pF	
			-	35 (-512 Q)	-	-	45 (-1024 Q)	-	pF	
Video line capacitance	CV	2 V bias	-	7 (-128 Q)	-	-	10 (-256 Q)	-	pF	
			-	11 (-256 Q)	-	-	16 (-512 Q)	-	pF	
			-	20 (-512 Q)	-	-	30 (-1024 Q)	-	pF	

*6: Vφ is input pulse voltage (refer to P.6 "Video bias voltage margin")

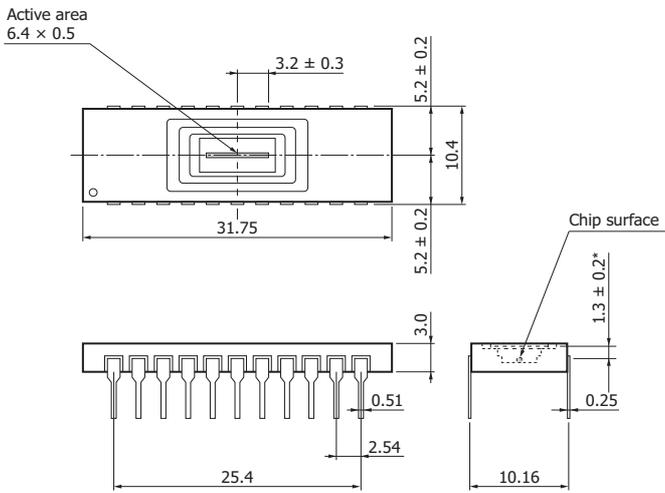
*7: trf is the clock pulse rise or fall time. A clock pulse space of "rise time/fall time - 20" ns (nanoseconds) or more should be input if the clock pulse rise or fall time is longer than 20 ns. (refer to P.6 "Timing chart for driver circuit")

*8: Vb=2.0 V, Vφ=5.0 V

*9: Measured with C7883 driver circuit.

Dimensional outlines (unit: mm)

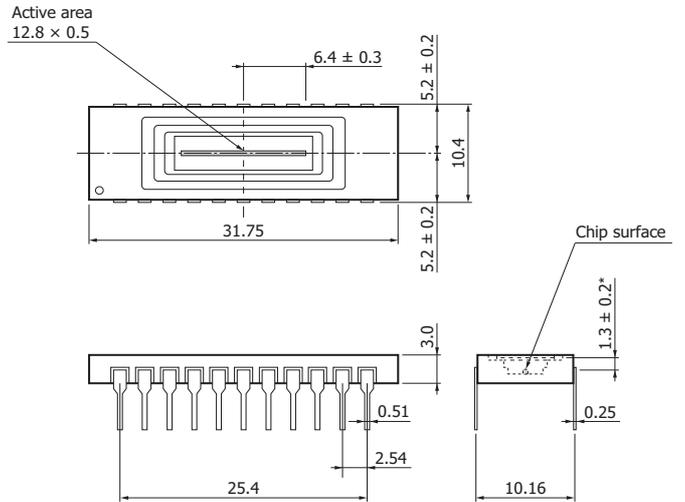
S3902-128Q, S3903-256Q



* Optical distance from the outer surface of the quartz window to the chip surface

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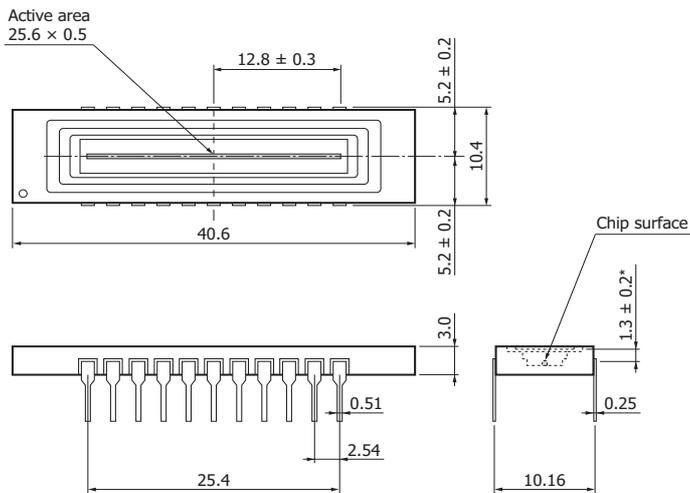
S3902-256Q, S3903-512Q



* Optical distance from the outer surface of the quartz window to the chip surface

KMPDA0109EB

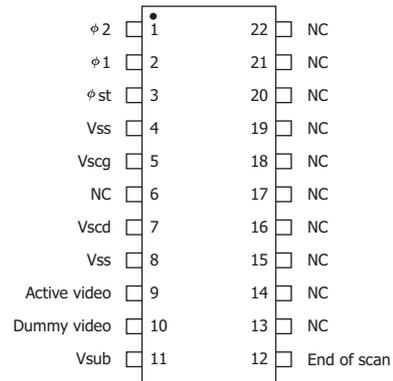
S3902-512Q, S3903-1024Q



* Optical distance from the outer surface of the quartz window to the chip surface

KMPDA0110EB

Pin connection

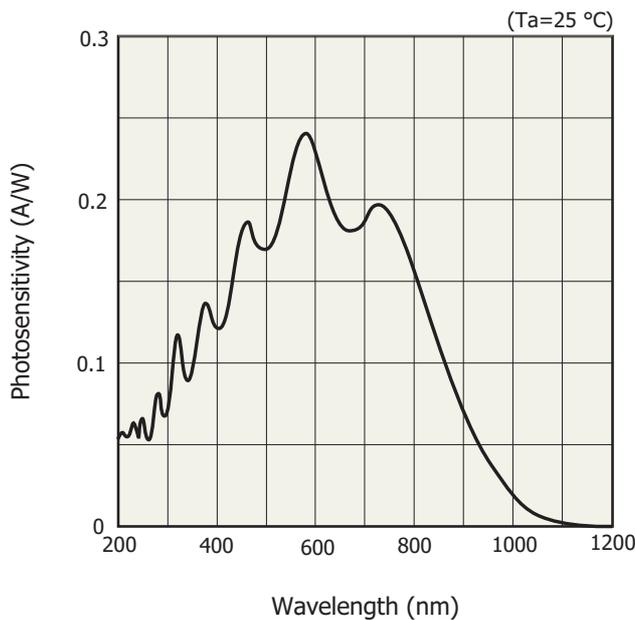


Vss, Vsub and NC should be grounded.

KMPDC0056EA

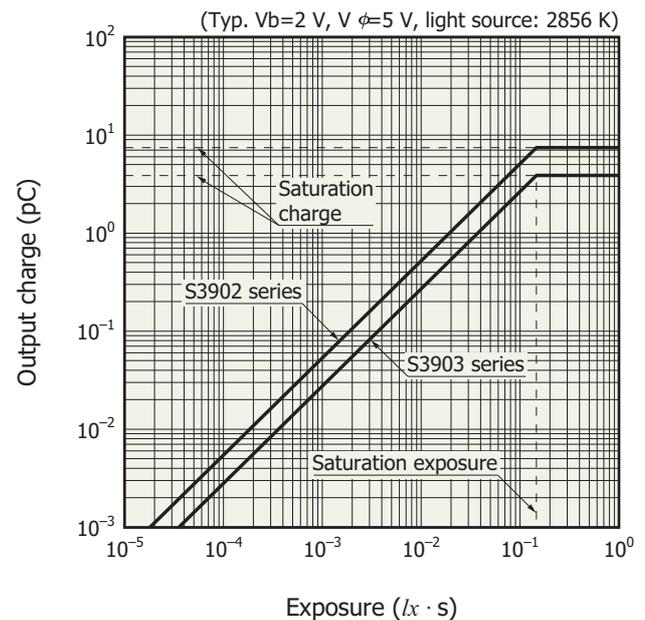
Terminal	Input or output	Description
$\phi 1, \phi 2$	Input (CMOS logic compatible)	Pulses for operating the MOS shift register. The video data rate is equal to the clock pulse frequency since the video output signal is obtained synchronously with the rise of $\phi 2$ pulse.
ϕst	Input (CMOS logic compatible)	Pulse for starting the MOS shift register operation. The time interval between start pulses is equal to the signal accumulation time.
Vss	-	Connected to the anode of each photodiode. This should be grounded.
Vscg	Input	Used for restricting blooming. This should be grounded.
Vscd	Input	Used for restricting blooming. This should be biased at a voltage equal to the video bias voltage.
Active video	Output	Video output signal. Connects to photodiode cathodes when the address is on. A positive voltage should be applied to the video line in order to use photodiodes with a reverse voltage. When the amplitude of $\phi 1$ and $\phi 2$ is 5 V, a video bias voltage of 2 V is recommended.
Dummy video	Output	This has the same structure as the active video, but is not connected to photodiodes, so only spike noise is output. This should be biased at a voltage equal to the active video or left as an open-circuit when not needed.
Vsub	-	Connected to the silicon substrate. This should be grounded.
End of scan	Output (CMOS logic compatible)	This should be pulled up at 5 V by using a 10 k Ω resistor. This is a negative going pulse that appears synchronously with the $\phi 2$ timing right after the last photodiode is addressed.
NC	-	Should be grounded.

Spectral response (typical example)



KMPDB0149EA

Output charge vs. exposure



KMPDB0117EA

■ Construction of image sensor

The NMOS image sensor consists of a scanning circuit made up of MOS transistors, a photodiode array, and a switching transistor array that addresses each photodiode, all integrated onto a monolithic silicon chip. "Equivalent circuit" (see P.1) shows the circuit of a NMOS linear image sensor.

The MOS scanning circuit operates at low power consumption and generates a scanning pulse train by using a start pulse and 2-phase clock pulses in order to turn on each address sequentially. Each address switch is comprised of an NMOS transistor using the photodiode as the source, the video line as the drain and the scanning pulse input section as the gate.

The photodiode array operates in charge integration mode so that the output is proportional to the amount of light exposure (light intensity × integration time).

Each cell consists of an active photodiode and a dummy photodiode, which are respectively connected to the active video line and the dummy video line via a switching transistor. Each of the active photodiodes is also connected to the saturation control drain via the saturation control transistor, so that the photodiode blooming can be suppressed by grounding the saturation control gate. Applying a pulse signal to the saturation control gate triggers all reset. (See P.8 "Auxiliary functions".)

"Active area structure" (see P.1) shows the schematic diagram of the photodiode active area. This active area has a PN junction consisting of an N-type diffusion layer formed on a P-type silicon substrate. A signal charge generated by light input accumulates as a capacitive charge in this PN junction. The N-type diffusion layer provides high UV sensitivity but low dark current.

■ Driver circuit

S3902/S3903 series do not require any DC voltage supply for operation. However, the Vss, Vsub and all NC terminals must be grounded. A start pulse ϕ_{st} and 2-phase clock pulses ϕ_1 , ϕ_2 are needed to drive the shift register. These start and clock pulses are positive going pulses and CMOS logic compatible.

The 2-phase clock pulses ϕ_1 , ϕ_2 can be either completely separated or complementary. However, both pulses must not be "High" at the same time.

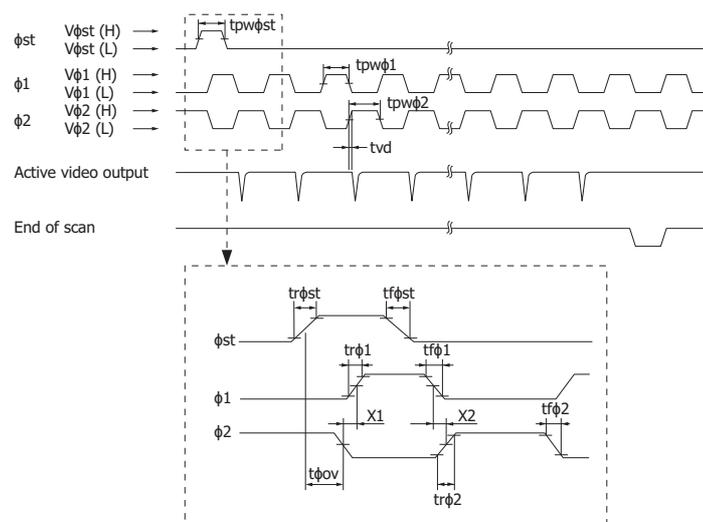
A clock pulse space (X1 and X2 in "Timing chart for driver circuit") of a "rise time/fall time - 20" ns or more should be input if the rise and fall times of ϕ_1 , ϕ_2 are longer than 20 ns. The ϕ_1 and ϕ_2 clock pulses must be held at "High" at least 200 ns. Since the photodiode signal is obtained at the rise of each ϕ_2 pulse, the clock pulse frequency will equal the video data rate.

The amplitude of start pulse ϕ_{st} is the same as the ϕ_1 and ϕ_2 pulses. The shift register starts the scanning at the "High" level of ϕ_{st} , so the start pulse interval determines the length of signal accumulation time. The ϕ_{st} pulse must be held "High" at least 200 ns and overlap with ϕ_2 at least for 200 ns. To operate the shift register correctly, ϕ_2 must change from the "High" level to the "Low" level only once during "High" level of ϕ_{st} . The timing chart for each pulse is shown in "Timing chart for driver circuit".

■ End of scan

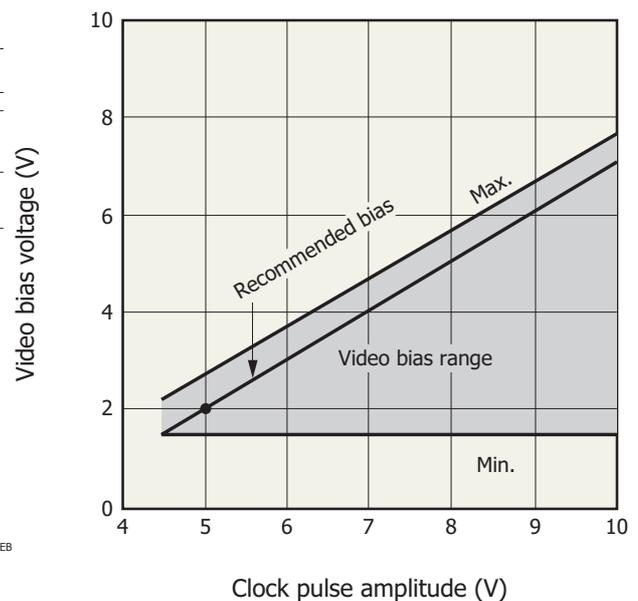
The end of scan (\overline{EOS}) signal appears in synchronization with the ϕ_2 timing right after the last photodiode is addressed, and the \overline{EOS} terminal should be pulled up at 5 V using a 10 k Ω resistor.

■ Timing chart for driver circuit



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■ Video bias voltage margin



KMPD80043EA

■ Signal readout circuit

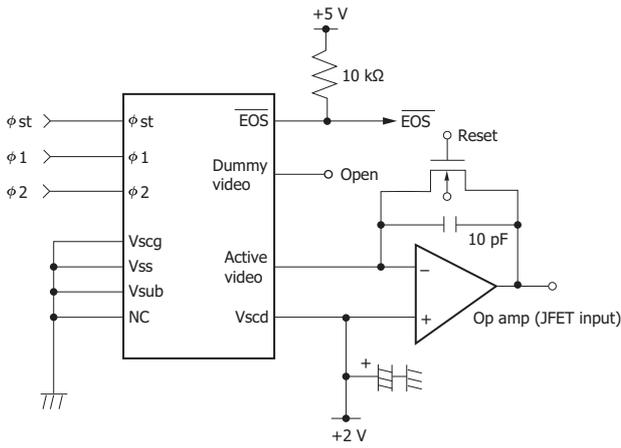
There are two methods for reading out the signal from an NMOS linear image sensor. One is a current detection method using the load resistance and the other is a current integration method using a charge amplifier. In either readout method, a positive bias must be applied to the video line because photodiode anodes of NMOS linear image sensors are set at 0 V (Vss). "Video bias voltage margin" (see P.6) shows a typical video bias voltage margin. As the clock pulse amplitude is higher, the video bias voltage can be set larger so the saturation charge can be increased. The rise and fall times of the video output waveform can be shortened if the video bias voltage is reduced while the clock pulse amplitude is still higher. When the amplitude of $\phi 1$, $\phi 2$ and ϕst is 5 V, setting the video bias voltage at 2 V is recommended.

To obtain good linearity, using the current integration method is advised. In this method, the integration capacitance is reset to the reference voltage level immediately before each photodiode is addressed and the signal charge is then stored as an integration capacitive charge when the address switch turns on. "Readout circuit example" and "Timing chart" show a typical current integration circuit and its pulse timing chart. To ensure stable output, the rise of a reset pulse must be delayed at least 50 ns from the fall of $\phi 2$.

Hamamatsu provides the following driver circuits and related products (sold separately).

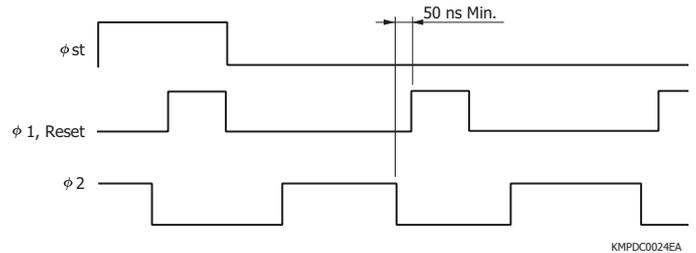
Product name	Type no.	Content	Feature
Driver circuit	C7884	Precision driver circuit	Low noise Good output linearity Boxcar waveform output
	C7884-01	High precision driver circuit	Ultra-low noise Good output linearity Boxcar waveform output

■ Readout circuit example



KMPDC0023EA

■ Timing chart



KMPDC0024EA

Output voltage V_{out} is

$$V_{out} [V] = \frac{\text{Output charge [C]}}{10 \times 10^{-12} [F]}$$
 shown in.

■ **Anti-blooming function**

If the incident light intensity is higher than the saturation charge level, even partially, a signal charge in excess of the saturation charge cannot accumulate in the photodiode. This excessive charge flows out into the video line degrading the signal purity. To avoid this problem and maintain the signal purity, applying the same voltage as the video bias voltage to the saturation control drain and grounding the saturation control gate are effective. If the incident light intensity is extremely high, a positive bias should be applied to the saturation control gate. The larger the voltage applied to the saturation control gate, the higher the function for suppressing the excessive saturation charge will be. However, this voltage also lowers the amount of saturation charge, so an optimum bias voltage should be selected.

■ **Auxiliary functions**

1) All reset

In normal operation, the accumulated charge in each photodiode is reset when the signal is read out. Besides this method that uses the readout line, S3902/S3903 series can reset the photodiode charge by applying a pulse to the saturation control gate. The amplitude of this pulse should be equal to the ϕ_1 , ϕ_2 and ϕ_{st} pulses and the pulse width should be longer than 5 μ s.

When the saturation control gate is set at the "High" level, all photodiodes are reset to the saturation control drain potential (equal to video bias). Conversely, when the saturation control gate is set at the "Low" level (0 V), the signal charge accumulates in each photodiode without being reset.

2) Dummy video

S3902/S3903 series have a dummy video line to eliminate spike noise contained in the video output waveform. Video signal with lower spike noise can be obtained by differential amplification applied between the active video line and dummy video line outputs. When not needed, leave this unconnected.

■ **Handling precautions**

1) Electrostatic countermeasures

NMOS linear image sensors are designed to resist static electrical charges. However, take sufficient cautions and countermeasures to prevent damage from static charges when handling the sensors.

2) Window

If dust or grime sticks to the surface of the light input window, it appears as a black blemish or smear on the image. Before using the image sensor, the window surface should be cleaned. Wipe off the window surface with a soft cloth, cleaning paper or cotton swab slightly moistened with organic solvent such as alcohol, and then lightly blow away with compressed air. Do not rub the window with dry cloth or cotton swab as this may generate static electricity.

■ **Related information**

www.hamamatsu.com/sp/ssd/doc_en.html

■ **Precautions**

- Disclaimer
- Image sensors

Information described in this material is current as of June 2017.

Product specifications are subject to change without prior notice due to improvements or other reasons. This document has been carefully prepared and the information contained is believed to be accurate. In rare cases, however, there may be inaccuracies such as text errors. Before using these products, always contact us for the delivery specification sheet to check the latest specifications.

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